FOUR-CHANNEL AUTOMOTIVE DIGITAL AMPLIFIERS

FEATURES

- **TAS5414A – Single-Ended Input**
- **TAS5424A – Differential Input**
- **Four-Channel Digital Power Amplifier**
- **Four Analog Inputs, Four BTL Power Outputs**
- **Typical Output Power per Channel at 10% THD+N**
  - **28 W/Ch Into 4 Ω at 14.4 Vdc**
  - **45 W/Ch Into 2 Ω at 14.4 Vdc**
  - **58 W/Ch Into 4 Ω at 21 Vdc**
  - **116 W/Ch Into 2 Ω at 21 Vdc PBTL**
- **Channels Can Be Paralleled (PBTL) for 1-Ω Applications**
- **THD+N < 0.02%, 1 kHz, 1 W Into 4 Ω**
- **Patented Pop- and Click-Reduction Technology**
  - **Soft Muting With Gain Ramp Control**
  - **Common-Mode Ramping**
- **Patented AM Interference Avoidance**
- **Patented Cycle-by-Cycle Current Limit**
- **75-dB PSRR**
- **Four-Address I^2C Serial Interface for Device Configuration and Control**
- **Configurable Channel Gains: 12-dB, 20-dB, 26-dB, 32-dB**
- **Load Diagnostic Functions:**
  - **Output Open and Shorted Load**
  - **Output-to-Power and -to-Ground Shorts**
  - **Patented Tweeter Detection**
- **Protection and Monitoring Functions:**
  - **Short-Circuit Protection**
  - **Load-Dump Protection to 50 V**
  - **Fortuitous Open Ground and Power Tolerant**
  - **Patented Output DC Level Detection While Music Playing**
  - **Overtemperature Protection**
  - **Over- and Undervoltage Conditions**
  - **Clip Detection**
- **36-Pin PSOP3 (DKD) Power SOP Package With Heat Slug Up for the TAS5414A**
- **44-Pin PSOP3 (DKD) Power SOP Package With Heat Slug Up for the TAS5424A**
- **64-Pin QFP (PHD) Power Package With Heat Slug Up for TAS5414A and TAS5424A**
- **Designed for Automotive EMC Requirements**
- **AECQ100 Compliant**
- **ISO9000:2002 TS16949 Certified**
- **–40°C to 105°C Ambient Temperature Range**

APPLICATIONS

- **High-Power OEM/Retail Head Units and Amplifier Modules Where Feature Densities and System Configurations Require Reduction in Heat From the Audio Power Amplifier**

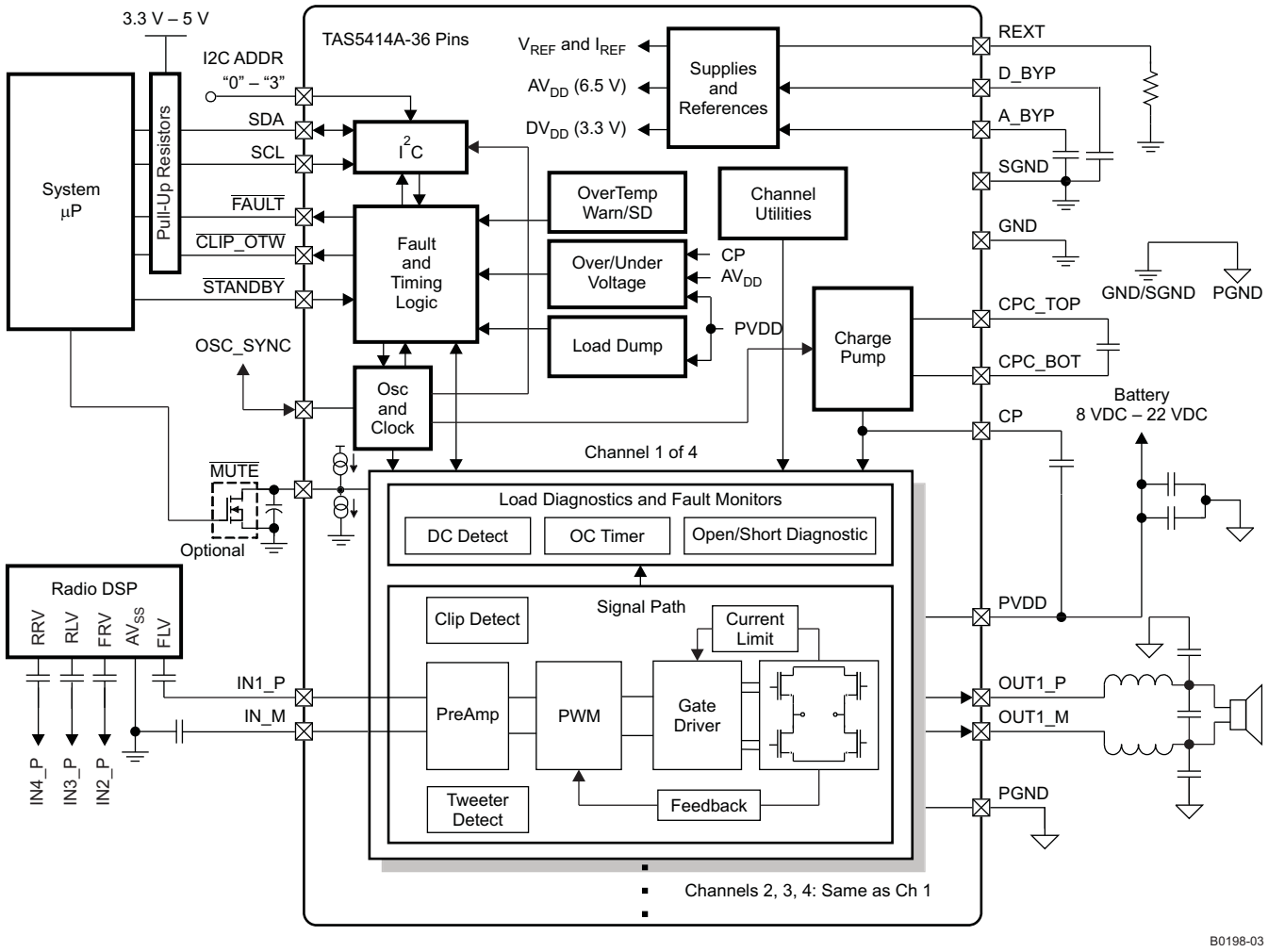
DESCRIPTION

The TAS5414A and TAS5424A are four-channel digital audio amplifiers designed for use in automotive head units and external amplifier modules. The TAS5414A and TAS5424A provide four channels at 23 W continuously into 4 Ω at less than 1% THD+N from a 14.4-V supply. Each channel can also deliver 38 W into 2 Ω at 1% THD+N. The TAS5414A uses single-ended analog inputs, while the TAS5424A employs differential inputs for increased immunity to common-mode system noise. The digital PWM topology of the TAS5414A and TAS5424A provides dramatic improvements in efficiency over traditional linear amplifier solutions. This reduces the power dissipated by the amplifier by a factor of ten under typical music playback conditions. High efficiency is accomplished without the need for complicated power-supply schemes. Multiple TAS5414As or TAS5424As can be synchronized to meet high-channel-count applications.

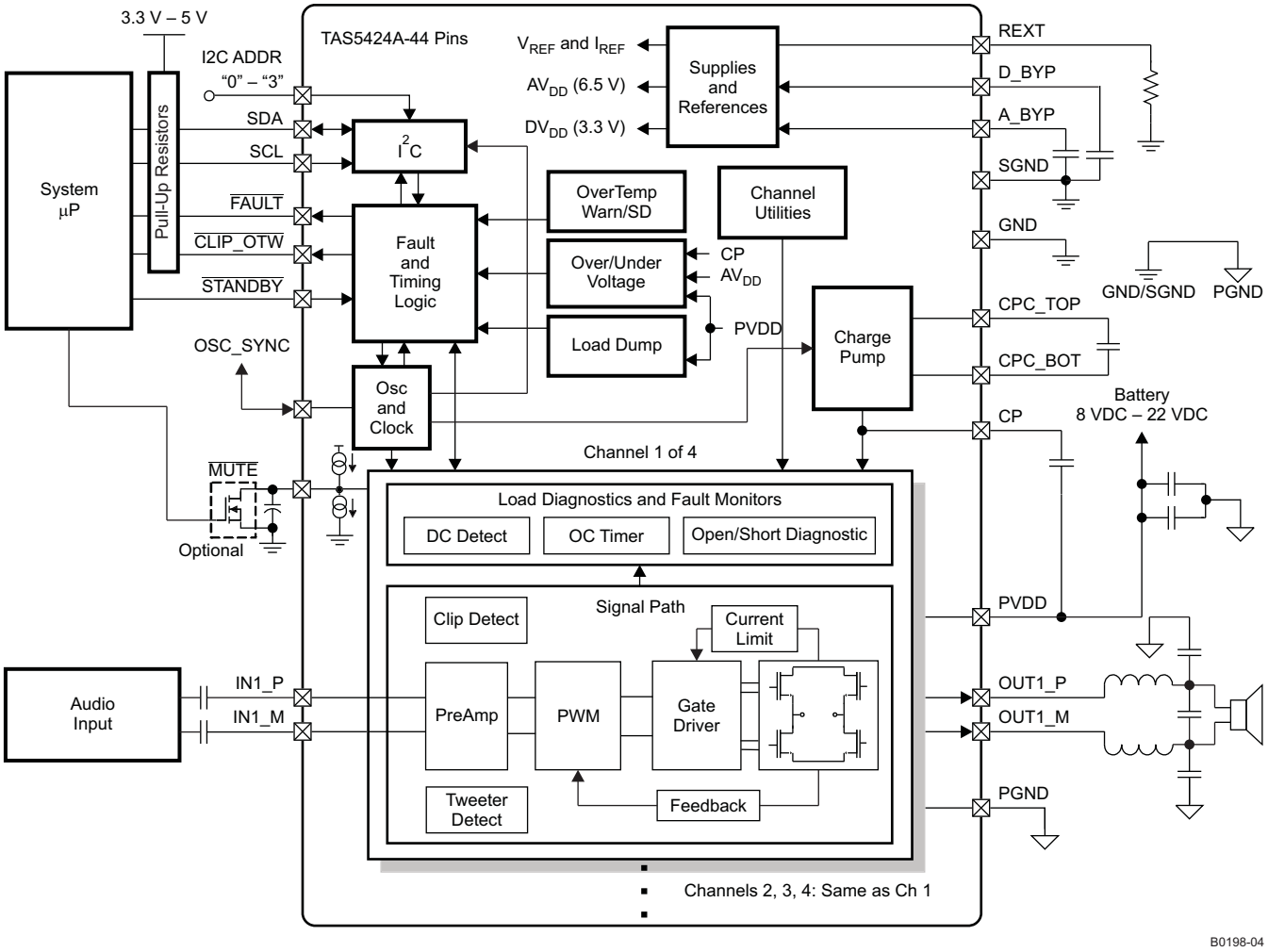
The TAS5414A and TAS5424A incorporate all the functionality needed to perform in the demanding OEM applications area. They have built-in load diagnostic functions for detecting and diagnosing misconnected outputs to help to reduce test time during the manufacturing process.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TAS5414A FUNCTIONAL BLOCK DIAGRAM



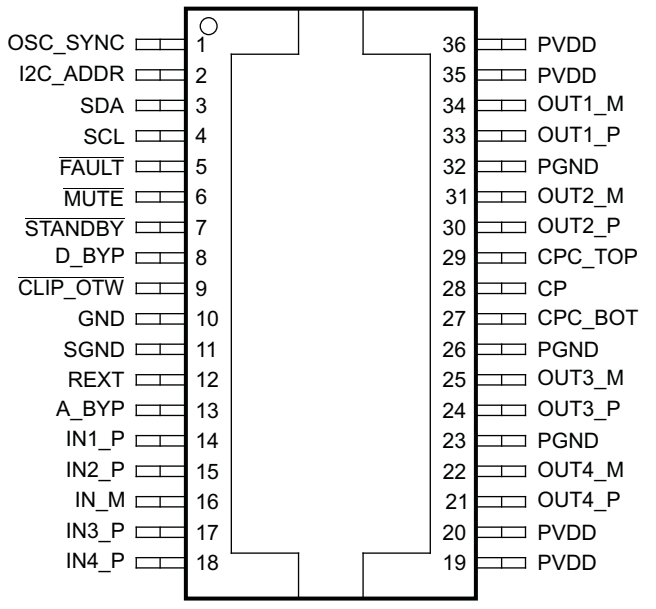
TAS5424A FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS AND FUNCTIONS

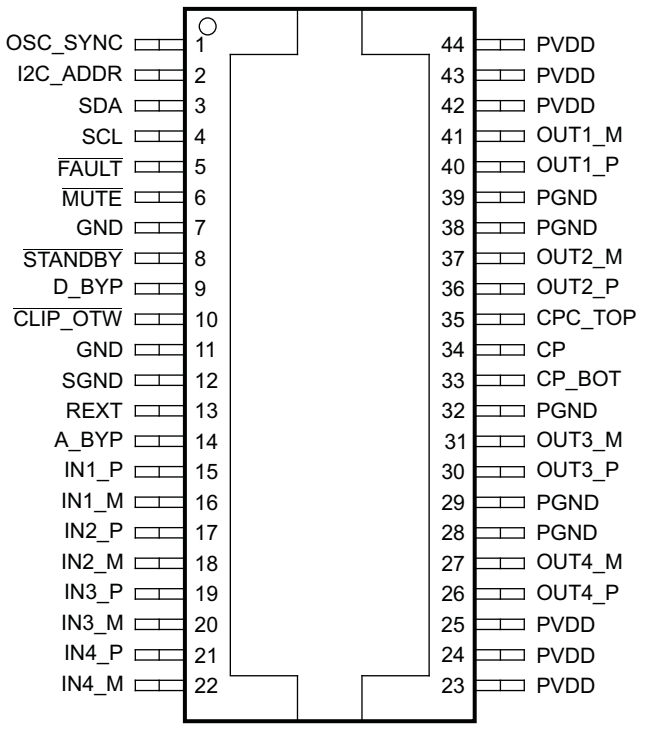
The pin assignments for the TAS5414A and TAS5424A are shown as follows.

TAS5414A
DKD Package
(Top View)



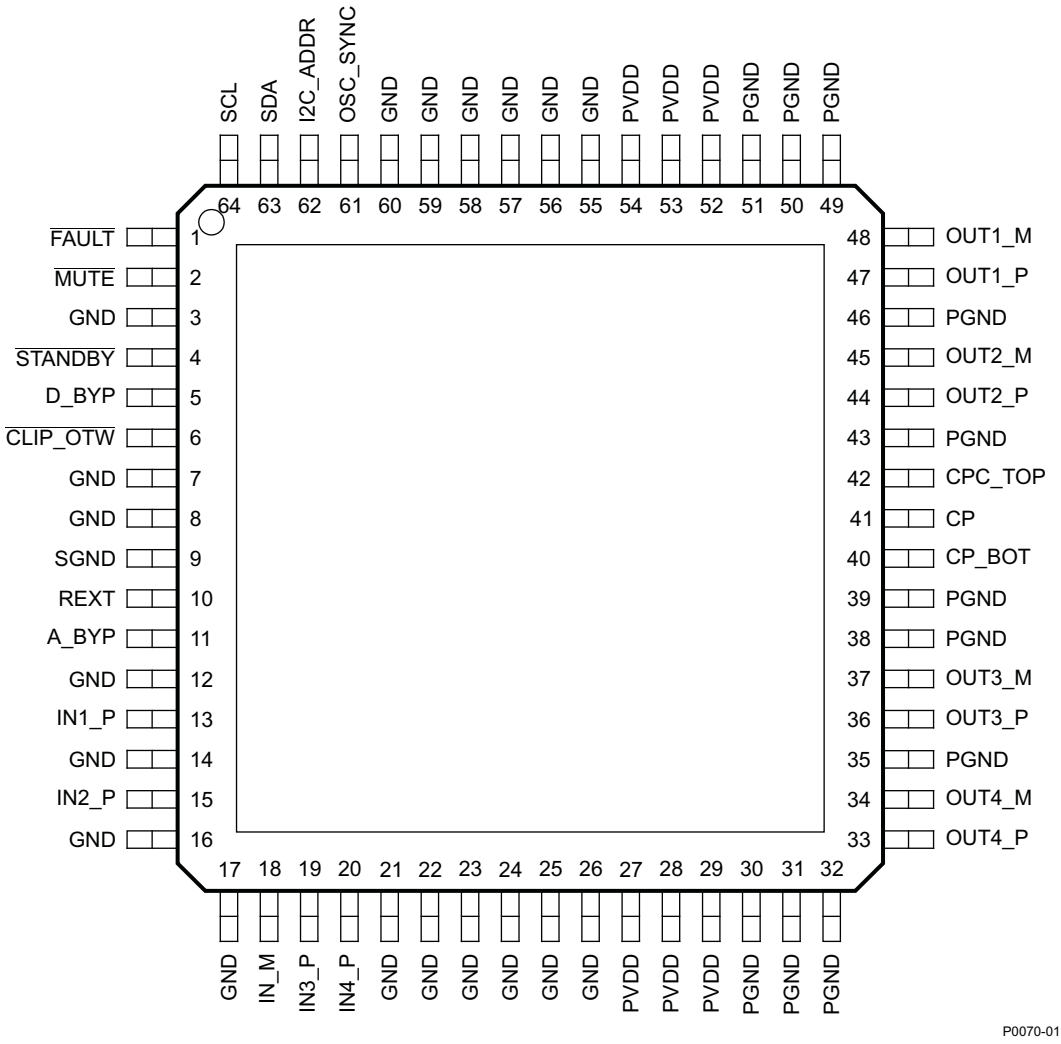
P0018-04

TAS5424A
DKD Package
(Top View)



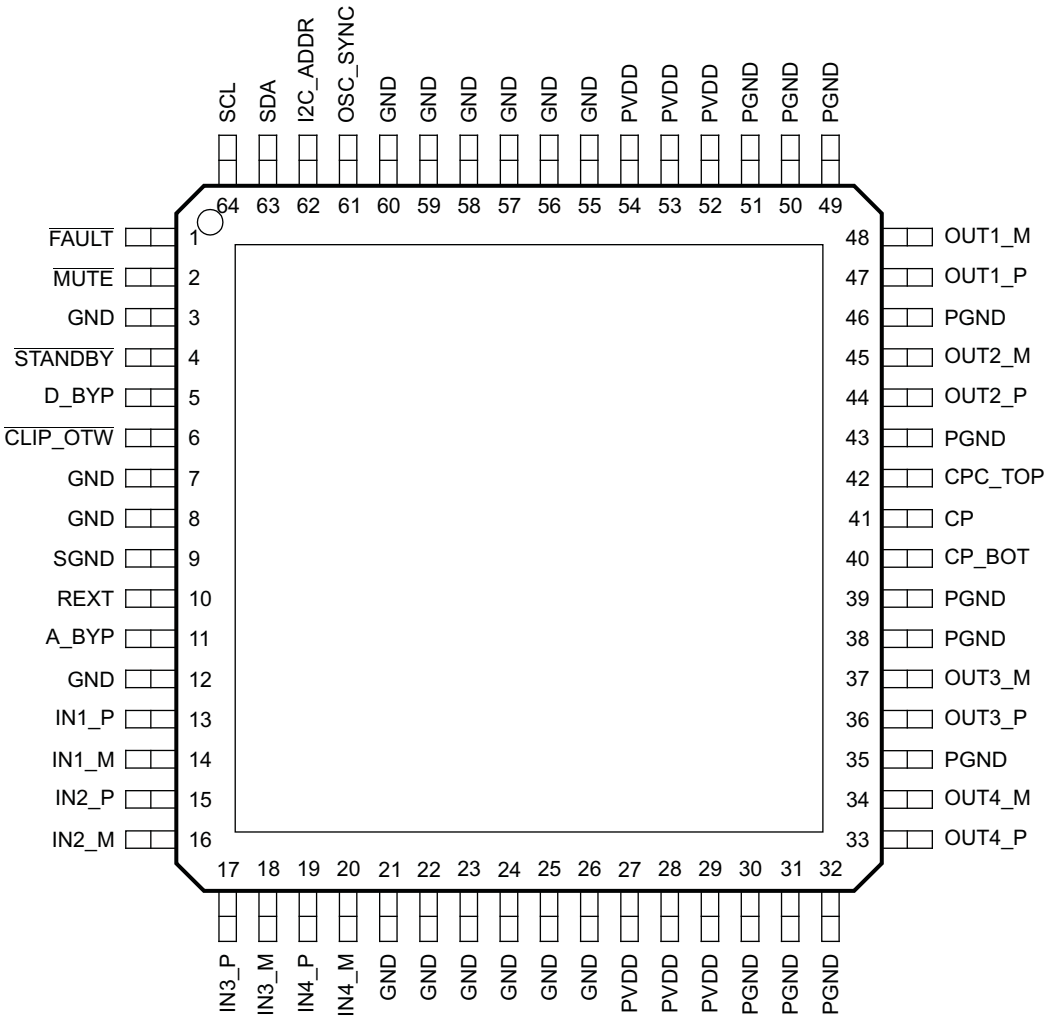
P0055-02

TAS5414A
PHD Package
(Top View)



P0070-01

TAS5424A
PHD Package
(Top View)



P0070-02

Table 1. TERMINAL FUNCTIONS

TERMINAL					TYPE[1]	DESCRIPTION
NAME	DKD Package		PHD Package			
	TAS5414A NO.	TAS5424A NO.	TAS5414A NO.	TAS5424A NO.		
A_BYP	13	14	11	11	PBY	Bypass capacitor for the AVDD analog regulator
$\overline{\text{CLIP\_OTW}}$	9	10	6	6	DO	Open-drain CLIP, OTW, or logical OR of the CLIP and OTW outputs. It also reports tweeter detection during tweeter mode.
CP	28	34	41	41	CP	Top of main storage capacitor for charge pump (bottom goes to PVDD)
CPC_BOT	27	33	40	40	CP	Bottom of flying capacitor for charge pump
CPC_TOP	29	35	42	42	CP	Top of flying capacitor for charge pump
D_BYP	8	9	5	5	PBY	Bypass pin for DVDD regulator output
$\overline{\text{FAULT}}$	5	5	1	1	DO	Global fault output (open drain): UV, OV, OTSD, OCSD, DC
GND	10	7, 11	3, 7, 8, 12, 14, 16, 17, 21, 22, 23, 24, 25, 26, 55, 56, 57, 58, 59, 60	3, 7, 8, 12, 14, 16, 17, 21, 22, 23, 24, 25, 26, 55, 56, 57, 58, 59, 60	DG	Ground
I2C_ADDR	2	2	62	62	AI	I^2C address bit
IN1_M	N/A	16	N/A	14	AI	Inverting analog input for channel 1 (TAS5424A only)
IN1_P	14	15	13	13	AI	Non-inverting analog input for channel 1
IN2_M	N/A	18	N/A	16	AI	Inverting analog input for channel 2 (TAS5424A only)
IN2_P	15	17	15	15	AI	Non-inverting analog input for channel 2
IN3_M	N/A	20	N/A	18	AI	Inverting analog input for channel 3 (TAS5424A only)
IN3_P	17	19	19	17	AI	Non-inverting analog input for channel 3
IN4_M	N/A	22	N/A	20	AI	Inverting analog input for channel 4 (TAS5424A only)
IN4_P	18	21	20	19	AI	Non-inverting analog input for channel 4
IN_M	16	N/A	18	N/A	ARTN	Signal return for the 4 analog channel inputs (TAS5414A only)
$\overline{\text{MUTE}}$	6	6	2	2	AI	Gain ramp control: mute (low), play (high)
OSC_SYNC	1	1	61	61	DI/DO	Oscillator sync input from master or output to slave amplifiers (20 MHz divided by 5, 6, or 7)
OUT1_M	34	41	48	48	PO	– polarity output for bridge 1
OUT1_P	33	40	47	47	PO	+ polarity output for bridge 1
OUT2_M	31	37	45	45	PO	– polarity output for bridge 2
OUT2_P	30	36	44	44	PO	+ polarity output for bridge 2
OUT3_M	25	31	37	37	PO	– polarity output for bridge 3
OUT3_P	24	30	36	36	PO	+ polarity output for bridge 3
OUT4_M	22	27	34	34	PO	– polarity output for bridge 4
OUT4_P	21	26	33	33	PO	+ polarity output for bridge 4
PGND	23, 26, 32	28, 29, 32, 38, 39	30, 31, 32, 35, 38, 39, 43, 46, 49, 50, 51	30, 31, 32, 35, 38, 39, 43, 46, 49, 50, 51	PGND	Power GND
PVDD	19, 20, 35, 36	23, 24, 25, 42, 43, 44	27, 28, 29, 52, 53, 54	27, 28, 29, 52, 53, 54	PWR	PVDD supply
REXT	12	13	10	10	AI	Precision resistor pin to set clock frequency
SCL	4	4	64	64	DI	I^2C clock input from system I^2C master

(1) DI = digital input, DO = digital output, AI = analog input, ARTN = analog signal return, PWR = power supply, PGND = power ground, PBY = power bypass, PO = power output, AG = analog ground, DG = digital ground, CP = charge pump.

Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL					TYPE(1)	DESCRIPTION
NAME	DKD Package		PHD Package			
	TAS5414A NO.	TAS5424A NO.	TAS5414A NO.	TAS5424A NO.		
SDA	3	3	63	63	DI/DO	I^2C data I/O for communication with system I^2C master
SGND	11	12	9	9	AG/DG	Signal ground (analog and digital signal ground)
$\overline{\text{STANDBY}}$	7	8	4	4	DI	Active-low STANDBY pin. Standby (low), power up (high)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
PVDD	DC supply voltage range	Relative to PGND	–0.3 to 30	V
$PVDD_{MAX}$	Pulsed supply voltage range	t ≤ 100 ms exposure	–1 to 50	V
$PVDD_{RAMP}$	Supply voltage ramp rate	Voltage rising up to $PVDD_{MAX}$	25	V/ms
I_{PVDD}	Externally imposed dc supply current per PVDD or PGND pin		±12	A
I_{PVDD_MAX}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms	17	A
I_O	Maximum allowed dc current per output pin		±13.5	A
I_{O_MAX}(1)	Pulsed output current per output pin (single pulse)	t < 100 ms	±17	A
I_{IN_MAX}	Maximum current, all digital and analog input pins(2)	DC or pulsed	±1	mA
I_{MUTE_MAX}	Maximum current on $\overline{\text{MUTE}}$ pin	DC or pulsed	±20	mA
I_{IN_ODMAX}	Maximum sinking current for open-drain pins		7	mA
V_{LOGIC}	Input voltage range for logic pin relative to SGND (SCL and SDA pins)	Supply voltage range: 6.5 V < PVDD < 24 V	–0.3 to 7	V
V_{I2C_ADDR}	Input voltage range for I2C_ADDR pin relative to SGND	Supply voltage range: 6.5 V < PVDD < 24 V	–0.3 to 7	V
$V_{STANDBY}$	Input voltage range for $\overline{\text{STANDBY}}$ pin	Supply voltage range: 6.5 V < PVDD < 24V	–0.3 to 5.8	V
V_{OSC_SYNC}	Input voltage range for OSC_SYNC pin relative to SGND	Supply voltage range: 6.5 V < PVDD < 24 V	–0.3 to 3.6	V
V_{AIN_MAX}	Maximum instantaneous input voltage (per pin), analog input pins	Supply voltage range: 6.5 V < PVDD < 24 V	6.5	V
$V_{AIN\_AC\_MAX\_5414}$	Maximum ac-coupled input voltage for TAS5414A(2), analog input pins	Supply voltage range: 6.5 V < PVDD < 24 V	1.9	Vrms
$V_{AIN\_AC\_MAX\_5424}$	Maximum ac-coupled differential input voltage for TAS5424A(2), analog input pins	Supply voltage range: 6.5 V < PVDD < 24 V	3.8 (1.9 per pin)	Vrms
V_{AIN_DC}	Input voltage range for analog pin relative to AGND (INx pins)	Supply voltage range: 6.5 V < PVDD < 24 V	–0.3 to 6.5	V
T_J	Maximum operating junction temperature range		–55 to 150	°C
T_{stg}	Storage temperature range		–55 to 150	°C
T_{SOLDER}	Lead temperature during soldering 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
Power dissipation	Continuous power dissipation	T_{case} = 70°C	80	W
V_{PGND}	Maximum voltage between PGND and GND		±0.3	V
V_{SGND}	Maximum voltage between SGND and GND		±0.3	V

(1) Pulsed current ratings are maximum survivable currents externally applied to the TAS5414A and TAS5424A. High currents may be encountered during reverse battery, fortuitous open ground, and fortuitous open supply fault conditions.
(2) See *Application Information* section for information on analog input voltage and ac coupling.

THERMAL CHARACTERISTICS

PARAMETER		VALUE (Typical)	UNIT
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance, DKD package	1	°C/W
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance, PHD package	1.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. See the *Thermal Information* section.	°C/W
	Exposed pad dimensions, DKD package	13.8×5.8	mm
	Exposed pad dimensions, PHD package	8×8	mm

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	TYP	MAX	UNIT
$PVDD_{OP}$	DC supply voltage range relative to PGND		8	14.4	22	V
$PVDD_{I2C}$	DC supply voltage range for I^2C reporting		6	14.4	26.5	V
V_{AIN_5414} (2)	Analog audio input signal level (TAS5414A)	AC-coupled input voltage	0		0.25–1(3)	Vrms
V_{AIN_5424} (2)	Analog audio input signal level (TAS5424A)	AC-coupled input voltage	0		0.5–2(3)	Vrms
f_{AUDIO_TW}	Audio frequency for tweeter detect		10	20	25	kHz
T_A	Ambient temperature		–40		105	°C
T_J	Junction temperature	An adequate heat sink is required to keep T_J within specified range.	–40		115	°C
R_L	Nominal speaker load impedance		2	4		Ω
V_{PU}	Pullup voltage supply (for open-drain logic outputs)		3	3.3 or 5	5.5	V
R_{PU_EXT}	External pullup resistor on open-drain logic outputs	Resistor connected between open-drain logic output and V_{PU} supply	10	50	100	kΩ
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	5	10	kΩ
R_{I2C_ADD}	Total resistance of voltage divider for I^2C address slave 1 or slave 2, connected between D_BYP and SGND pins		10		100	kΩ
R_{REXT}	External resistance on REXT pin	1% tolerance required	19.8	20	20.2	kΩ
C_{D_BYP}	External capacitance on D_BYP pin		10		120	nF
C_{A_BYP}	External capacitance on A_BYP pin		10		120	nF
C_{IN}	External capacitance to analog input pin in series with input signal			1		µF
C_{FLY}	Flying capacitor on charge pump		0.47	1	1.5	µF
C_P	Charge pump capacitor		0.47	1	1.5	µF
C_{MUTE}	Capacitance on MUTE pin		3.3	330		nF
$C_{OSCSYNC\_MAX}$	Allowed loading capacitance on OSC_SYNC pin			5		pF

(1) The *Recommended Operating Conditions* table specifies only that the device is functional in the given range. See the *Electrical Characteristics* table for specified performance limits.
(2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB
(3) Maximum recommended input voltage is determined by the gain setting.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, Rext = 20 kΩ, master mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All four channels running in MUTE mode		240	300	mA
I_{PVDD_Hi-Z}		All four channels in Hi-Z mode		80		
I_{PVDD_STBY}	PVDD standby current	STANDBY mode, $T_J \le 85°C$		2	20	µA
OUTPUT POWER						
P_{OUT}	Output power per channel	4 Ω, PVDD = 14.4 V, THD+N ≤ 1%, 1 kHz, T_c = 75°C		23		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	25	28		
		4 Ω, PVDD = 14.4 V, square wave, 1 kHz, T_c = 75°C		43		
		4 Ω, PVDD = 21 V, THD+N = 1%, 1 kHz, T_c = 75°C		47		
		4 Ω, PVDD = 21 V, THD+N = 10%, 1 kHz, T_c = 75°C	50	58		
		2 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T_c = 75°C		38		
		2 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	40	45		
		2 Ω, PVDD = 14.4 V, square wave 1 kHz, T_c = 75°C		70		
		PBTL 2-Ω operation, PVDD = 21 V, THD+N = 10%, 1 kHz, T_c = 75°C		116		
		PBTL 1-Ω operation, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C		90		
EFF_P	Power efficiency	4 channels operating, 23-W output power/ch, L = 10 µH, $T_J \le 85°C$		90%		
AUDIO PERFORMANCE						
V_{NOISE}	Noise voltage at output	G = 26 dB, zero input, AES17 filter, and A-weighting		60	100	µV
Crosstalk	Channel crosstalk	1 W, G = 26 dB, 1 kHz	60	75		dB
$CMRR_{5424}$	Common-mode rejection ratio (TAS5424A)	1 kHz, 1 Vrms referenced to SGND, G = 26 dB	60	75		dB
PSRR	Power supply rejection ratio	G = 26 dB, PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz	60	75		dB
THD+N	Total harmonic distortion + noise	P = 1 W, G = 26 dB, f = 1 kHz, 0°C ≤ T_J ≤ 75°C		0.02%	0.1%	
f_S	Switching frequency	Switching frequency selectable for AM interference avoidance	336	357	378	kHz
			392	417	442	
			470	500	530	
R_{AIN}	Analog input resistance	Internal shunt resistance on each input pin	60	80	100	kΩ
V_{IN_CM}	Common-mode input voltage (non-clipping)	AC-coupled common-mode input voltage (zero differential input)			1.3	Vrms
V_{CM_INT}	Internal common-mode input bias voltage	Internal bias applied to IN_M pin		3.25		V
G	Voltage gain (V_O/V_{IN})	Source impedance = 0 Ω	11	12	13	dB
			19	20	21	
			25	26	27	
			31	32	33	
G_{CH}	Channel-to-channel variation	Any gain commanded	–1	0	1	dB
t_{CM}	Output-voltage common-mode ramping time			35		ms
t_{GAIN}	Gain ramping time	External C_{MUTE} = 330 nF		30		ms
PWM OUTPUT STAGE						
R_{DSon}	FET drain-to-source resistance	Not including bond wire resistance, T_J = 25°C		75	95	mΩ
V_{O_OFFSET}	Output offset voltage	Zero input signal and G = 26 dB		±10	±25	mV
PVDD OVERVOLTAGE (OV) PROTECTION						
V_{OV}	PVDD overvoltage shutdown		22.1	23.7	26.3	V
LOAD DUMP (LD) PROTECTION						
$V_{LD\_SD\_SET}$	Load-dump shutdown voltage		26.6	29	32	V
$V_{LD\_SD\_CLEAR}$	Recovery voltage for load-dump shutdown		23.5	26.4	28.4	V
PVDD UNDERVOLTAGE (UV) PROTECTION						
V_{UV_SET}	PVDD undervoltage shutdown		6.5	7	7.5	V
V_{UV_CLEAR}	Recovery voltage for PVDD UV		7	7.5	8	V

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, Rext = 20 kΩ, master mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AVDD						
V_{A_BYP}	A_BYP pin voltage			6.5		V
$V_{A\_BYP\_UV\_SET}$	A_BYP UV voltage			4.8		V
$V_{A\_BYP\_UV\_CLEAR}$	Recovery voltage A_BYP UV			5.3		V
DVDD						
V_{D_BYP}	D_BYP pin voltage			3.3		V
POWER-ON RESET (POR)						
V_{POR}	Maximum PVDD voltage for POR; I^2C active above this voltage				6	V
V_{POR_HY}	PVDD recovery hysteresis voltage for POR			0.1		V
REXT						
V_{REXT}	Rext pin voltage			1.24		V
CHARGE PUMP (CP)						
V_{CPUV_SET}	CP undervoltage			4.8		V
V_{CPUV_CLEAR}	Recovery voltage for CP UV			5.2		V
OVERTEMPERATURE (OV) PROTECTION						
T_{OTW1_CLEAR}	Junction temperature for overtemperature warning		102	115	128	°C
T_{OTW1_SET} / T_{OTW2_CLEAR}			112	125	138	
T_{OTW2_SET} / T_{OTW3_CLEAR}			122	135	148	
T_{OTW3_SET} / T_{OTWD_CLEAR}			132	145	158	
T_{OTSD}	Junction temperature for overtemperature shutdown		142	155	168	
CURRENT LIMITING PROTECTION						
I_{LIM1}	Current limit 1 (load current)	Load < 4 Ω	5.5	7.3	9	A
I_{LIM2}	Current limit 2 (load current), I^2C setting current limit level 2	Load < 2 Ω	8.5	11	13.5	A
OVERCURRENT (OC) SHUTDOWN PROTECTION						
I_{MAX1}	Maximum current 1 (peak output current)	Any short to supply, ground, or other channels	9.5	11.3	13	A
I_{MAX2}	Maximum current 2 (peak output current)		11.5	14.3	17	A
TWEETER DETECT						
I_{TH_TW}	Load current threshold for tweeter detect		325	540	750	mA
I_{LIM_TW}	Load current limit for tweeter detect			2		A
STANDBY MODE						
V_{IH_STBY}	$\overline{\text{STANDBY}}$ input voltage for logic-level high		2		5.5	V
V_{IL_STBY}	$\overline{\text{STANDBY}}$ input voltage for logic-level low		0		0.7	V
I_{STBY_PIN}	$\overline{\text{STANDBY}}$ pin current			0.1	0.2	µA
MUTE MODE						
G_{MUTE}	Output attenuation	$\overline{\text{MUTE}}$ pin ≤ 0.9 Vdc, V_{IN} = 1 Vrms on all inputs		85		dB
DC DETECT						
$V_{TH\_DCD\_POS}$	DC detect positive threshold default value	PVDD = 14.4 Vdc, register 0x0E = 8EH		6.5		V
$V_{TH\_DCD\_NEG}$	DC detect negative threshold default value	PVDD = 14.4 Vdc, register 0x0F = 3DH		–6.5		V
t_{DCD}	DC detect step response time for four channels				4.3	s
CLIP_OTW REPORT						
$V_{OH\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
$V_{OL\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level low (open-drain logic output)				0.5	V

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, Rext = 20 kΩ, master mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DELAY\_CLIPDET}$	$\overline{CLIP\_OTW}$ signal delay when output clipping detected				20	µs
FAULT REPORT						
V_{OH_FAULT}	$\overline{FAULT}$ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
V_{OL_FAULT}	$\overline{FAULT}$ pin output voltage for logic-level low (open-drain logic output)				0.5	V
OPEN/SHORT DIAGNOSTICS						
R_{S2P}, R_{S2G}	Maximum resistance to detect a short from OUT pin(s) to PVDD or ground				200	Ω
R_{OPEN_LOAD}	Minimum load resistance to detect open circuit	Including speaker wires	300	800	1300	Ω
$R_{SHORTED\_LOAD}$	Maximum load resistance to detect short circuit	Including speaker wires	0.5	1	1.5	Ω
I^2C ADDRESS DECODER						
$t_{LATCH\_I2CADDR}$	Time delay to latch I^2C address after POR			300		µs
V_{I2C_ADDR}	Voltage on I2C_ADDR pin for address 0	Connect to SGND	0%	0%	15%	V_{D_BYP}
	Voltage on I2C_ADDR pin for address 1	External resistors in series between D_BYP and SGND as a voltage divider	25%	35%	45%	
	Voltage on I2C_ADDR pin for address 2		55%	65%	75%	
	Voltage on I2C_ADDR pin for address 3	Connect to D_BYP	85%	100%	100%	
I^2C						
t_{HOLD_I2C}	Power-on hold time before I^2C communication	$\overline{STANDBY}$ high		1		ms
f_{SCL}	SCL clock frequency				100	kHz
V_{IH_SCL}	SCL pin input voltage for logic-level high	R_{PU_I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL_SCL}	SCL pin input voltage for logic-level low		–0.5		1.1	V
V_{OH_SDA}	SDA pin output voltage for logic-level high	I^2C read, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.4			V
V_{OL_SDA}	SDA pin output voltage for logic-level low	I^2C read, 3-mA sink current	0		0.4	V
V_{IH_SDA}	SDA pin input voltage for logic-level high	I^2C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL_SDA}	SDA pin input voltage for logic-level low	I^2C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	–0.5		1.1	V
C_i	Capacitance for SCL and SDA pins				10	pF
OSCILLATOR						
$V_{OH\_OSCSYNC}$	OSC_SYNC pin output voltage for logic-level high	I2C_ADDR pin set to MASTER mode	2.4		3.6	V
$V_{OL\_OSCSYNC}$	OSC_SYNC pin output voltage for logic-level low				0.5	V
$V_{IH\_OSCSYNC}$	OSC_SYNC pin input voltage for logic-level high	I2C_ADDR pin set to SLAVE mode	2		3.6	V
$V_{IL\_OSCSYNC}$	OSC_SYNC pin input voltage for logic-level low				0.8	V
f_{OSC_SYNC}	OSC_SYNC pin clock frequency	I2C_ADDR pin set to MASTER mode, f_S = 500 kHz, maximum capacitive loading = 5 pF	3.76	4.0	4.24	MHz
		I2C_ADDR pin set to MASTER mode, f_S = 417 kHz, maximum capacitive loading = 5 pF	3.13	3.33	3.63	
		I2C_ADDR pin set to MASTER mode, f_S = 357 kHz, maximum capacitive loading = 5 pF	2.68	2.85	3.0	

TIMING REQUIREMENTS FOR I²C INTERFACE SIGNALS

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_r	Rise time for both SDA and SCL signals			1000	ns
t_f	Fall time for both SDA and SCL signals			300	ns
$t_{w(H)}$	SCL pulse duration, high	4			µs
$t_{w(L)}$	SCL pulse duration, low	4.7			µs
t_{su2}	Setup time for START condition	4.7			µs
t_{h2}	START condition hold time after which first clock pulse is generated	4			µs
t_{su1}	Data setup time	250			ns
t_{h1}	Data hold time	0(1)			ns
t_{su3}	Setup time for STOP condition	4			µs
C_B	Load capacitance for each bus line			400	pF

(1) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

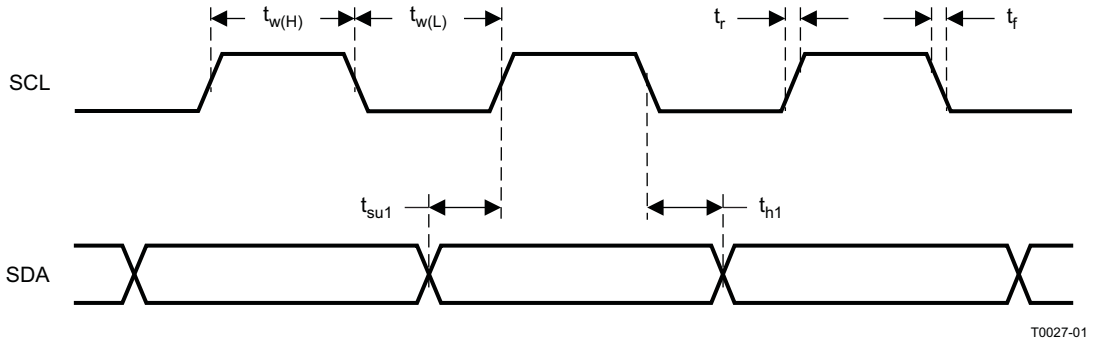


Figure 1. SCL and SDA Timing

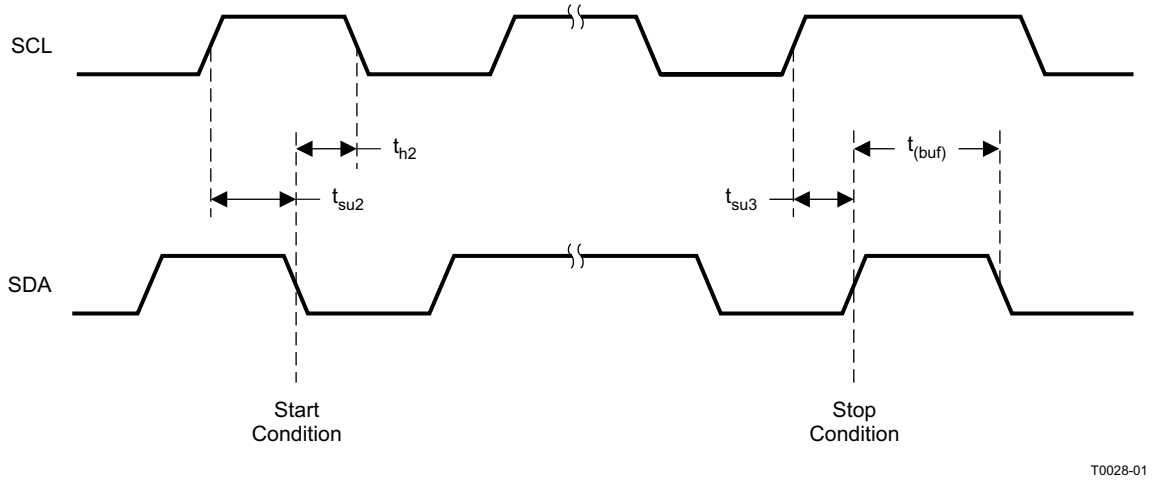


Figure 2. Timing for Start and Stop Conditions

TYPICAL CHARACTERISTICS

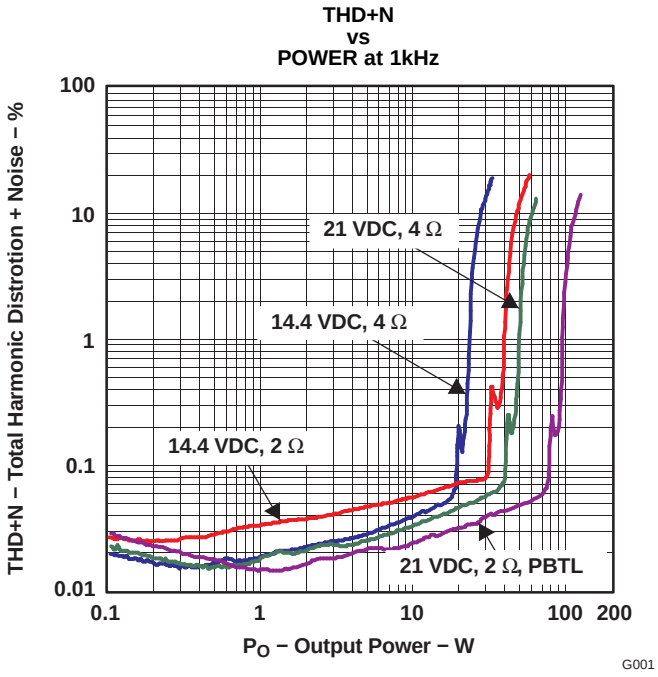


Figure 3.

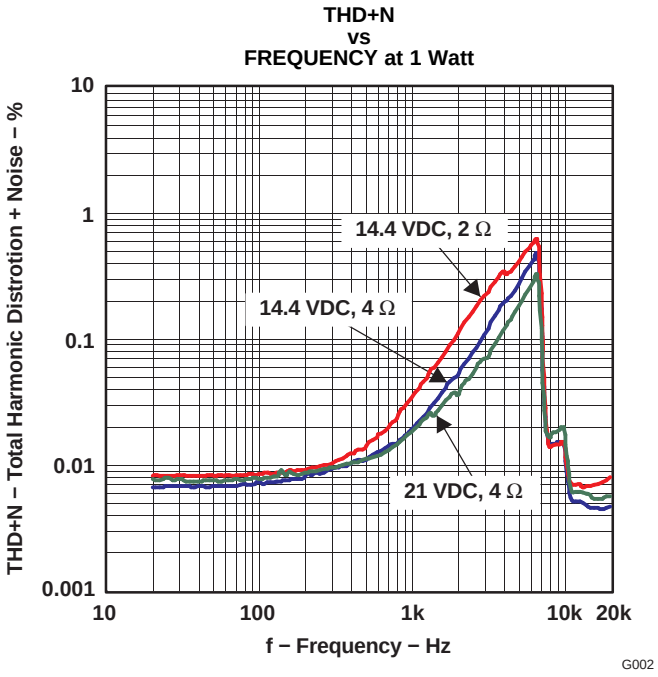


Figure 4.

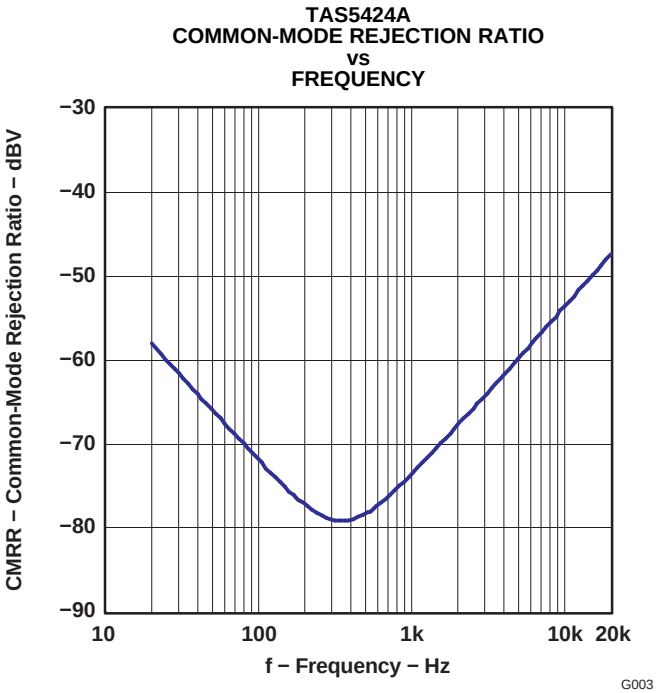


Figure 5.

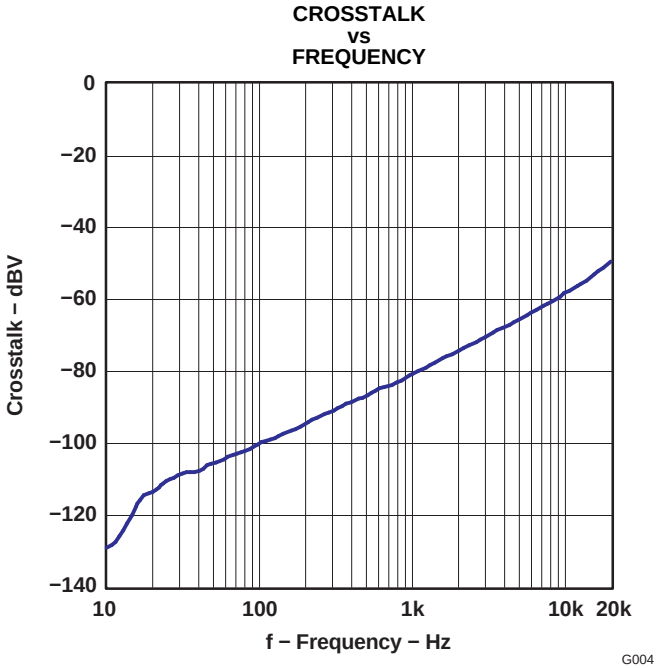


Figure 6.

TYPICAL CHARACTERISTICS (continued)

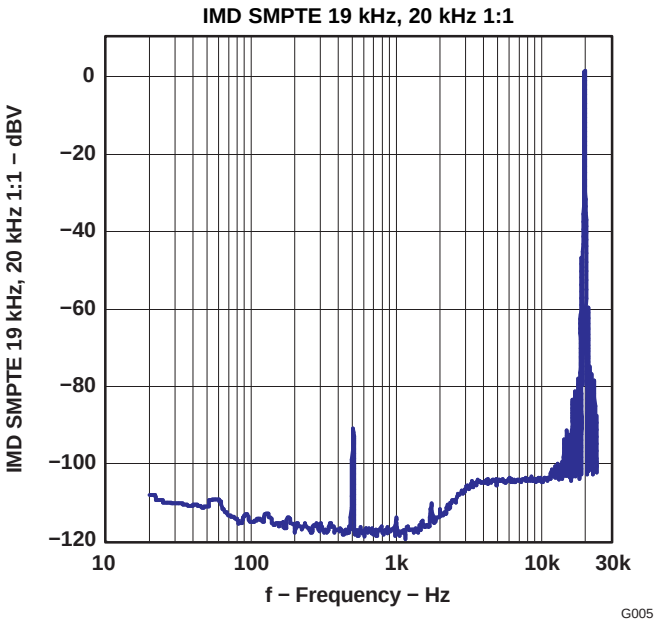


Figure 7.

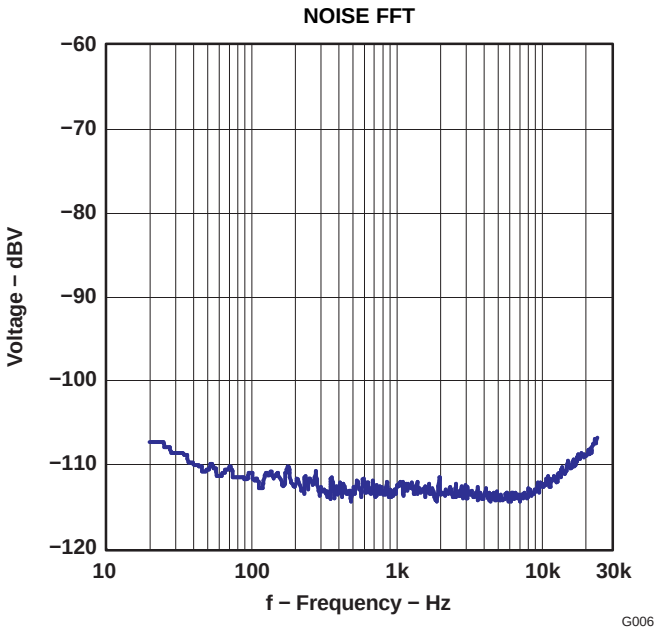


Figure 8.

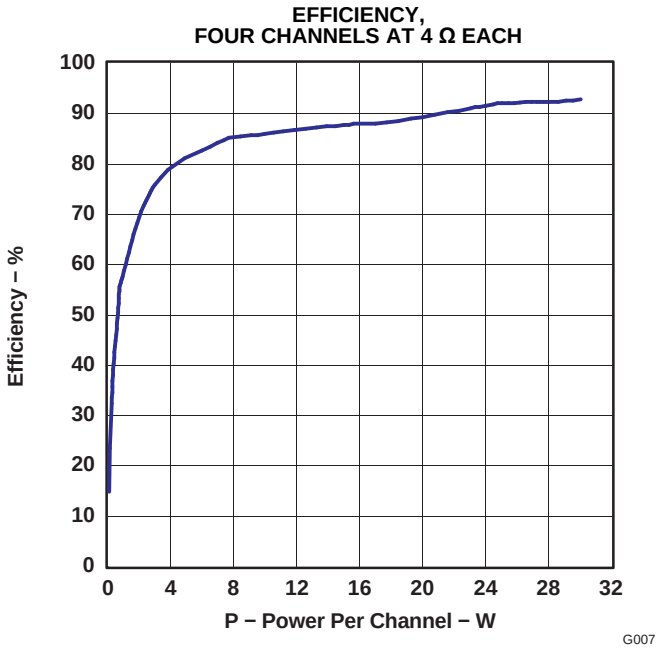


Figure 9.

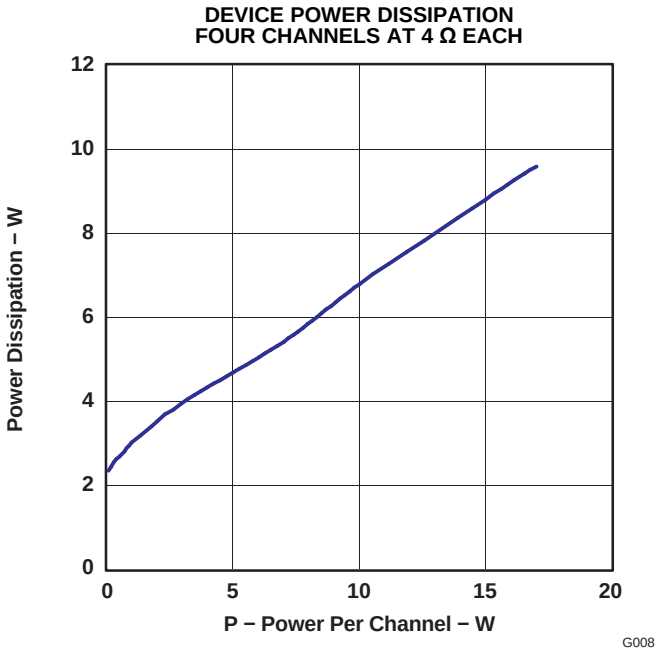


Figure 10.

TYPICAL CHARACTERISTICS (continued)

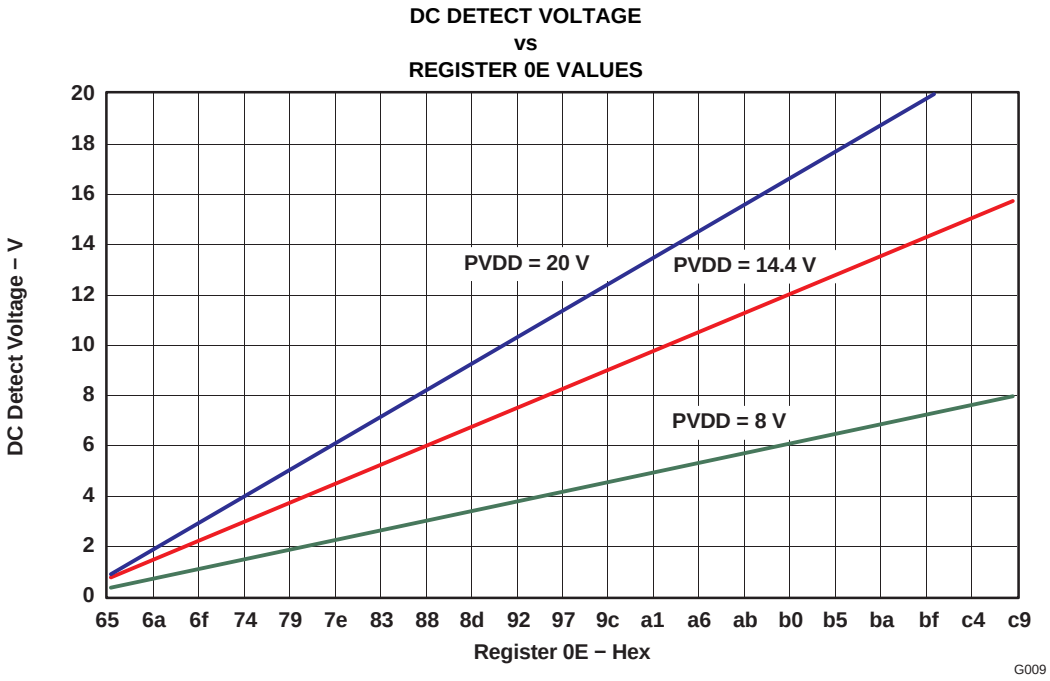


Figure 11.

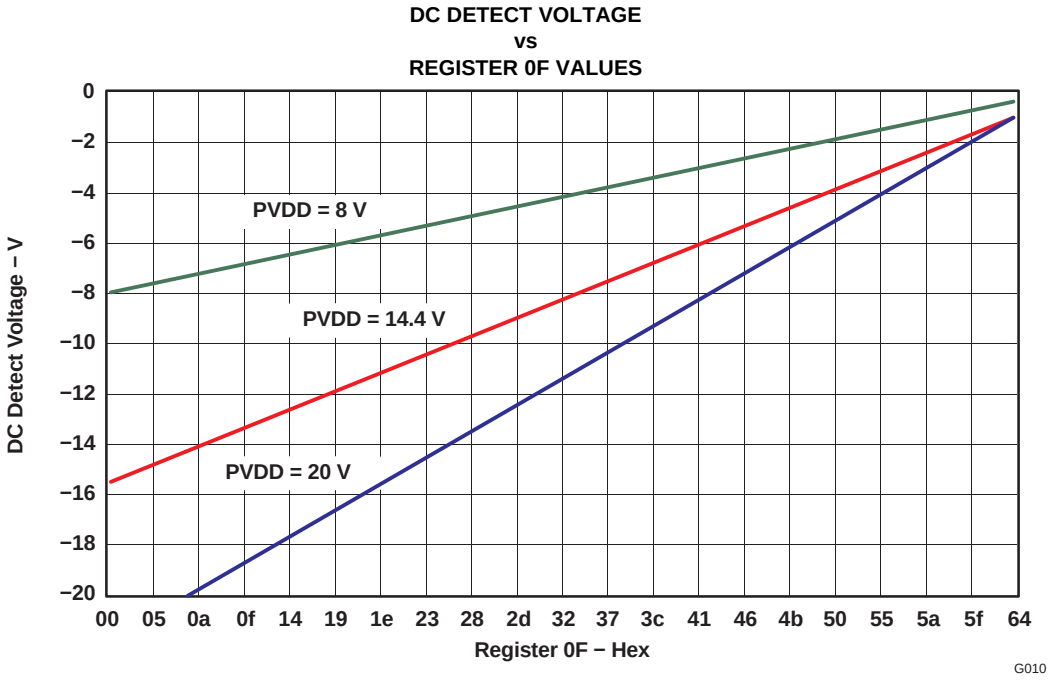


Figure 12.

DESCRIPTION OF OPERATION

OVERVIEW

The TAS5414A and TAS5424A are single-chip, four-channel, analog-input audio amplifiers for use in the automotive environment. The design uses an ultra-efficient class-D technology developed by Texas Instruments, but with changes needed by the automotive industry. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The TAS5414A and TAS5424A realize an audio sound system design with smaller size and lower weight than traditional class-AB solutions.

The TAS5414A and TAS5424A are composed of eight elements:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

Preamplifier

The preamplifier of the TAS5414A and TAS5424A is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance of the TAS5414A and TAS5424A allows the use of low-cost 1-µF input capacitors while still achieving extended low-frequency response. The preamplifier is powered by a dedicated, internally regulated supply, which gives it excellent noise immunity and channel separation. Also included in the preamp are:

1. **Mute Pop-and-Click Control**—An audio input signal is reshaped and amplified as a step when a mute is applied at the crest or trough of the signal. Such a step is perceived as a loud click. This is avoided in the TAS5414A and TAS5424A by ramping the gain gradually when a mute or play command is received. Another form of click and pop can be caused by the start or stopping of switching in a class-D amplifier. The TAS5414A and TAS5424A incorporate a patented method to reduce the pop energy during the switching startup and shutdown sequence. Fault conditions require rapid protection response by the TAS5414A and the TAS5424A, which do not have time to ramp the gain down in a pop-free manner. The device transitions into Hi-Z mode when an OV, UV, OC, OT, or DC fault is encountered. Also, activation of the $\overline{\text{STANDBY}}$ pin may not be pop-free.
2. **Gain Control**—The four gain settings are set in the preamplifier via I^2C control registers. The gain is set outside of the global feedback resistors of the TAS5414A and the TAS5424A, thus allowing for stability in the system under all load conditions and gain settings.
3. **DC Offset Reduction Circuitry**—Circuitry has been incorporated to reduce the dc offset. DC offset in high-gain amplifiers can produce audible clicks and pops when the amplifier is started or stopped. The offset reduction circuitry can be disabled or enabled via I^2C.

Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TAS5414A and TAS5424A, the modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0–100% modulation capability. The patented PWM uses clipping recovery circuitry to eliminate the deep saturation characteristic of PWMs when the input signal exceeds the modulator waveform.

Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high-current, full-bridge, power FET stage. The TAS5414A and TAS5424A use patent-pending techniques to avoid shoot-through and are optimized for EMI and audio performance.

Power FETs

The BTL output for each channel comprises four rugged N-channel 30-V FETs, each of which has an R_{DSon} of 75 mΩ for high efficiency and maximum power transfer to the load. These FETs are designed to handle large voltage transients during load dump.

Load Diagnostics

The TAS5414A and TAS5424A incorporate load diagnostic circuitry designed to help pinpoint the nature of output misconnections during installation. The TAS5414A and the TAS5424A include functions for detecting and determining the status of output connections. The following diagnostics are supported:

- Short to GND
- Short to PVDD
- Short across load (R < 1 Ω, typical)
- Open load (R > 800 Ω, typical)
- Tweeter detection

The presence of any of the short or open conditions is reported to the system via I^2C register read. The tweeter detect status can be read from the $\overline{\text{CLIP\_OTW}}$ pin when properly configured.

1. **Output Short and Open Diagnostics**—The TAS5414A and TAS5424A contain circuitry designed to detect shorts and open conditions on the outputs. The load diagnostic function can only be invoked when the output is in the Hi-Z mode. There are four phases of test during load diagnostics and two levels of test. In the full level, all channels must be in the Hi-Z state. All four phases are tested on each channel, all four channels at the same time. When fewer than four channels are in Hi-Z, the reduced level of test is the only available option. In the reduced level, only short to PVDD and short to GND can be tested. Load diagnostics can occur at power up before the amplifier is moved out of Hi-Z mode. If the amplifier is already in play mode, it must *Mute* and then *Hi-Z* before the load diagnostic can be performed. By performing the mute function, the normal pop- and click-free transitions occur before the diagnostics begin. The diagnostics are performed as shown in Figure 13. Figure 14 shows the impedance ranges for the open-load and shorted-load diagnostics. The results of the diagnostic are read from the diagnostic register for each channel via I^2C. **Note:** Do not send a command via I^2C to register 0x0C during the load diagnostic test.

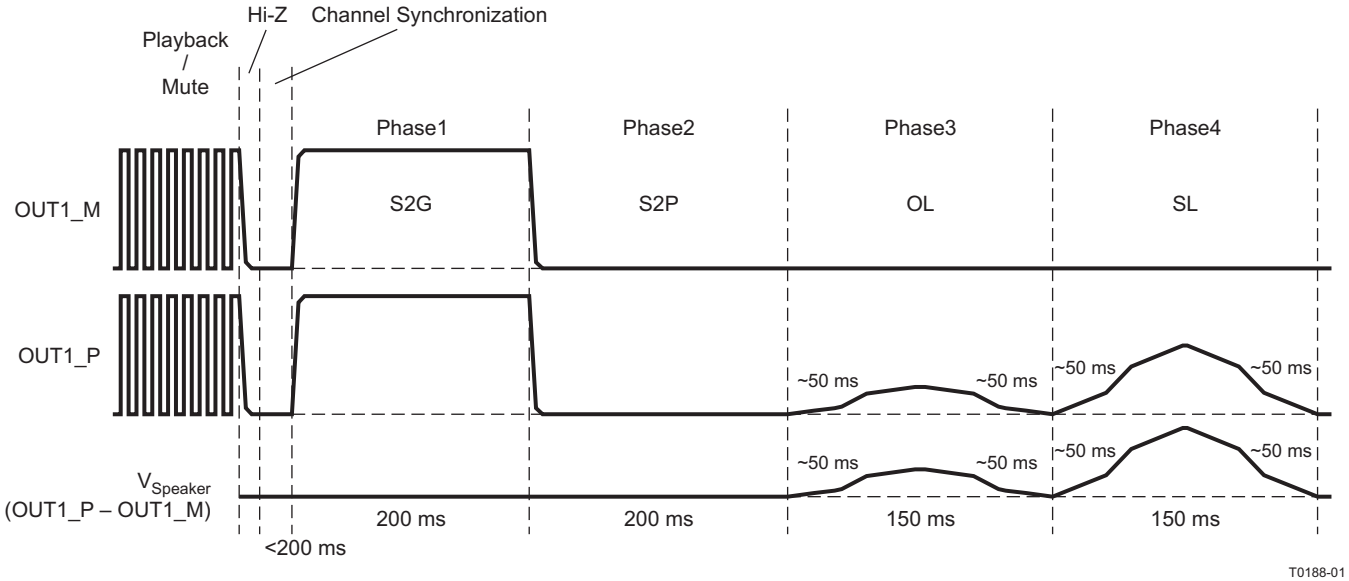


Figure 13. Load Diagnostics Sequence of Events

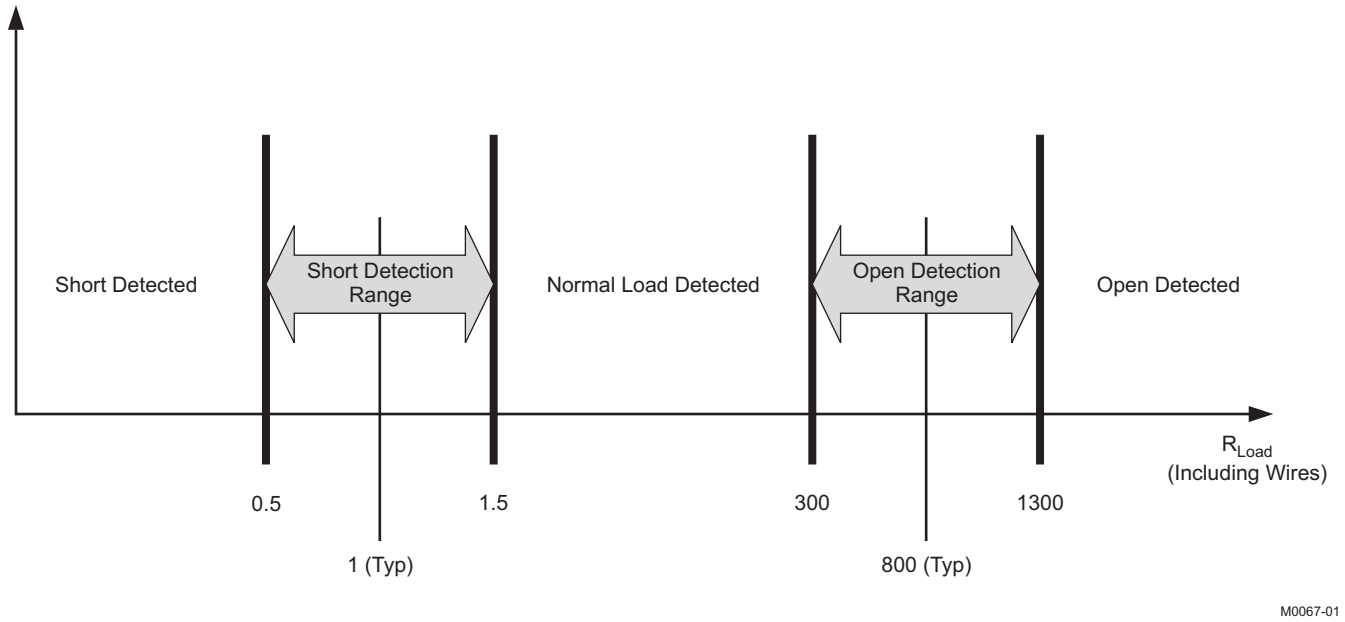


Figure 14. Open and Shorted Load Detection

2. **Tweeter Detection**—The tweeter detection function is an ac diagnostic used to determine proper connection of the tweeter when a passive crossover is used. The proper implementation of this diagnostic function is dependent on the amplitude of a user-supplied test signal and on the impedance vs frequency curve of the acoustic package. The tweeter function is invoked via I^2C, and all four channels should be tested individually. The tweeter detection uses the average cycle-by-cycle current limit circuit (see *CBC* section) to measure the current to the load. The current level for the tweeter detection threshold is typically 550 mA. The system (external to the TAS5414A and TAS5424A) must generate a tone burst in the 10-kHz to 25-kHz range. If the tone burst employs a frequency higher than 20 kHz, and if a sufficiently smooth amplitude ramp is used, the tweeter detection signal is silent. The frequency and amplitude of this tone burst must be calibrated by the user to result in a current draw greater than the selected threshold level when the tweeter is present. The tweeter detection results are monitored on the $\overline{\text{CLIP\_OTW}}$ pin during the application of the test tone. If the current threshold is attained during measurement, the tweeter is present; then the $\overline{\text{CLIP\_OTW}}$ pin is asserted. When the tweeter detector is activated, pulses on the $\overline{\text{CLIP\_OTW}}$ pin begin to toggle at 250 kHz to 500 kHz. As the detection signal gets stronger due to higher load current, the density (or duty cycle) of the pulses increases.

Protection and Monitoring

1. **Cycle-By-Cycle Current Limit (CBC)**—The CBC current-limiting circuit terminates each PWM pulse to limit the output current flow when the average current limit (I_{LIM}) threshold is exceeded. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, where power is temporarily limited at the peaks of the musical signal and normal operation continues without disruption when the overload is removed. The TAS5414A and TAS5424A do not prematurely shut down in this condition. All four channels continue in play mode and pass signal.
2. **Overcurrent Shutdown (OCSD)**—Under severe short-circuit events, such as a short to PVDD or ground, a peak-current detector is used, and the affected channel shuts down in 200 µs to 390 µs if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels are shut down in such a scenario. The user may restart the affected channel via I^2C. An OCSD event activates the fault pin, and the affected channel(s) are recorded in the I^2C fault register. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.
3. **DC Detect**—This circuit detects a dc offset continously during normal operation at the output of the amplifier. If the dc offset reaches the level defined in the I^2C registers for the specified time period, the circuit triggers. By default a dc detection event does not shut the output down. The shutdown function can be enabled or

disabled via I^2C. If enabled, the triggered channel shuts down, but the others remain playing and the $\overline{\text{FAULT}}$ pin is asserted. The positive dc level and negative dc level are defined in I^2C registers and can have separate thresholds.

4. **Clip Detect**—The clip detect circuit alerts the user to the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, a signal is passed to the $\overline{\text{CLIP\_OTW}}$ pin and it is asserted until the 100% duty-cycle PWM signal is no longer present. All four channels are connected to the same $\overline{\text{CLIP\_OTW}}$ pin. Through I^2C, the $\overline{\text{CLIP\_OTW}}$ signal can be changed to clip-only, OTW-only, or both. A fourth mode, used only during diagnostics, is the option to report tweeter detection events on this pin (see the *Tweeter Detection* section). The microcontroller in the system can monitor the signal at the $\overline{\text{CLIP\_OTW}}$ pin and may be configured to reduce the volume to all four channels in an active clipping-prevention circuit.
5. **Overtemperature Warning (OTW) and Overtemperature Shutdown (OTSD)**—By default, the $\overline{\text{CLIP\_OTW}}$ pin is set to indicate an OTW. This can be changed via I^2C commands. If selected to indicate a temperature warning, the $\overline{\text{CLIP\_OTW}}$ pin is asserted when the die temperature reaches 125°C. The OTW has three temperature thresholds with a 10°C hysteresis. Each threshold is indicated in I^2C register 0x04 bits 5, 6, and 7. The TAS5414A and TAS5424A still function until the temperature reaches the OTSD threshold. 155°C, at which time the outputs are placed into Hi-Z mode and the $\overline{\text{FAULT}}$ pin is asserted. I^2C is still active in the event of an OTSD and the registers can be read for faults, but all audio ceases abruptly. The OTSD resets at 145°C, to allow the TAS5414A/5424 to be turned back on through I^2C. The OTW is still indicated until the temperature drops below 115°C. All temperatures are nominal values.
6. **Undervoltage (UV) and Power-on-Reset (POR)**—The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the $\overline{\text{FAULT}}$ pin is asserted and the I^2C register is updated, depending on which voltage caused the event. Power-on-reset (POR) occurs when PVDD drops low enough. A POR event causes the I^2C to go into a high-impedance state. After the device recovers from the POR event, the device must be re-initialized via I^2C.
7. **Overvoltage (OV) and Load Dump**—The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the $\overline{\text{FAULT}}$ pin is asserted and the I^2C register is updated. If the voltage increases beyond the load dump threshold of 29 Vdc, the device shuts down and must be restarted once the voltage returns to a safe value. After the device recovers from the ≈ load dump event, the device must be re-initialized via I^2C. The TAS5414A and TAS5424A can withstand 50-V load-dump voltage spikes (see Figure 15). Also depicted in this graph are the voltage thresholds for normal operation region, overvoltage operation region, and load-dump protection region. Figure 13 shows the regions of operating voltage and the profile of the load dump event. Battery charger voltages from 25 V to 35 V can be withstood for up to 1 hour.

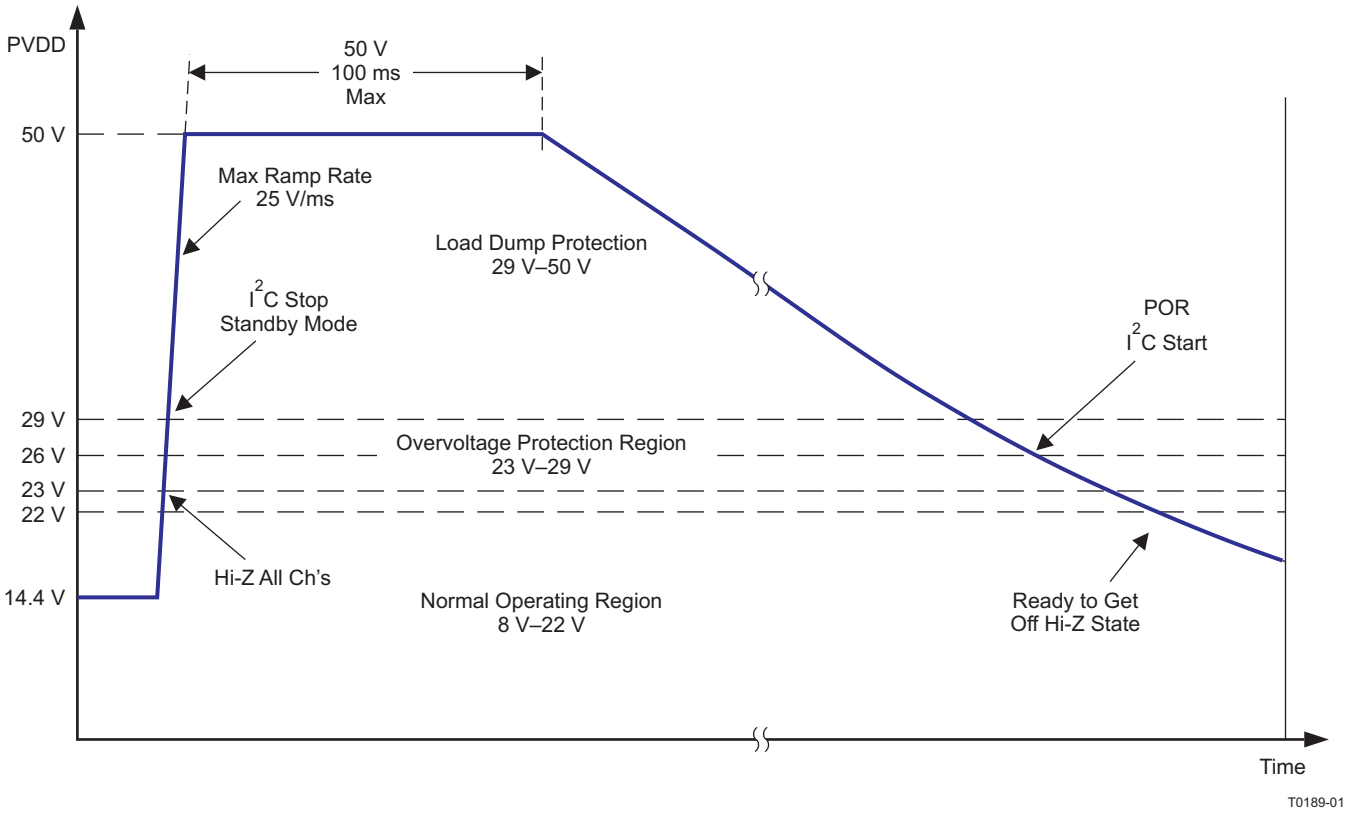


Figure 15. Voltage Operating Regions With Load Dump Transition Defined

Power Supply

The power for the device is most commonly provided by a car battery that can have a large voltage swing, 8 Vdc to 18 Vdc. PVDD is a filtered battery voltage, and it is the supply for the output FETS and the low-side FET gate driver. The high-side FET gate driver is supplied by a charge pump (CP) supply. The charge pump supplies the gate drive voltage for all four channels. The analog circuitry is powered by AVDD, which is a provided by an internal linear regulator. A 0.1µF/10V external bypass capacitor is needed at the A_BYP pin for this supply. It is recommended that no external components except the bypass capacitor be attached to this pin. The digital circuitry is powered by DVDD, which is provided by an internal linear regulator. A 0.1µF/10V external bypass capacitor is needed at the D_BYP pin. It is recommended that no external components except the bypass capacitor be attached to this pin.

The TAS5414A and TAS5424A can withstand fortuitous open ground and power conditions. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs. The uniqueness of the diagnostic capabilities allows the speakers and speaker wires to be debugged, eliminating the need to remove the amplifier to diagnose the problem.

I²C Serial Communication Bus

The TAS5414A and TAS5424A communicate with the system processor via the I²C serial communication bus. The TAS5414A and TAS5424A are I²C slave-only devices. The processor can poll the TAS5414A and the TAS5424A via I²C to determine the operating status of the device. All fault conditions and detections are reported via I²C. There are also numerous features and operating conditions that can be set via I²C.

The I²C bus allows control of the following configurations:

- Independent gain control of each channel. The gain can be set to 12 dB, 20 dB, 26 dB, and 32 dB.
- Select current limit (for 2-Ω and for 4-Ω loads). This allows optimal design of the filter inductor, and the use of smaller gauge speaker wires for 4-Ω applications.

- Select AM non-interference switching frequency
- Select the function of OTW_CLIP pin
- Enable or disable dc detect function with selectable threshold
- Place channel in Hi-Z (switching stopped) mode (mute)
- Select tweeter detect, set detect threshold and initiate function
- Initiate open/short load diagnostic
- Reset faults and return to normal switching operation from Hi-Z mode (unmute)

In addition to the standard SDA and SCL pins for the I^2C bus, the TAS5414A and the TAS5424A include a single pin that allows up to four devices to work together in a system with no additional hardware required for communication or synchronization. The I2C_ADDR pin sets the device in master or slave mode and selects the I^2C address for that device. Tie I2C_ADDR to DGND for master, to 1.2 Vdc for slave 1, to 2.4 Vdc for slave 2, and to D_BYP for slave 3. The OSC_SYNC pin is used to synchronize the internal clock oscillators and thereby avoid beat frequencies. An external oscillator can also be applied to this pin for external control of the switching frequency.

Table 2. Table 7. I2C_ADDR Pin Connection

DESCRIPTION	I2C_ADDR PIN CONNECTION	I^2C ADDRESS
TAS5414A/5424 0 (OSC MASTER)	To SGND pin	0xD8/D9
TAS5414A/5424 1 (OSC SLAVE1)	35% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDA/DB
TAS5414A/5424 2 (OSC SLAVE2)	65% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDC/DD
TAS5414A/5424 3 (OSC SLAVE3)	To D_BYP pin	0xDE/DF

(1) R_{I2C_ADDR} with 5% or better tolerance is recommended.

I^2C Bus Protocol

The TAS5414A and TAS5424A have a bidirectional serial control interface that is compatible with the Inter IC (I^2C) bus protocol and supports 100-kbps data transfer rates for random and sequential write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 16. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The TAS5414A and TAS5424A hold SDA LOW during the acknowledge-clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

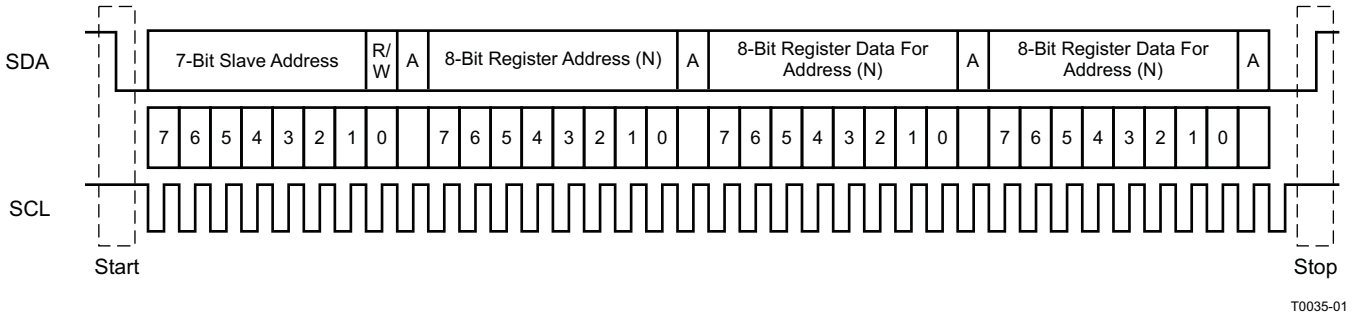


Figure 16. Typical I²C Sequence

Use the I2C_ADDR pin (pin 2) to program the device for one of four addresses. These four addresses are licensed I²C addresses and do not conflict with other licensed I²C audio devices. To communicate with the TAS5414A and the TAS5424A, the I²C master uses addresses shown in Figure 16. Read and write data can be transmitted using single-byte or multiple-byte data transfers.

Random Write

As shown in Figure 17, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the TAS5414A or TAS5424A device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the TAS5414A or TAS5424A again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5414A or TAS5424A again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

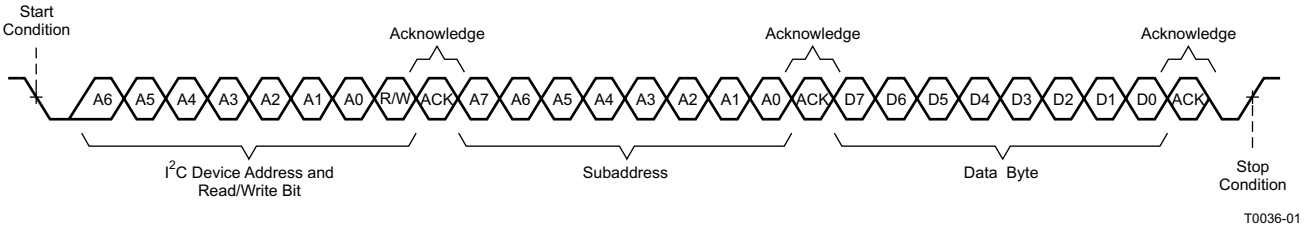


Figure 17. Random Write Transfer

Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master device to TAS5414A or TAS5424A as shown in Figure 17. After receiving each data byte, the TAS5414A or TAS5424A responds with an acknowledge bit and the I²C subaddress is automatically incremented by one.

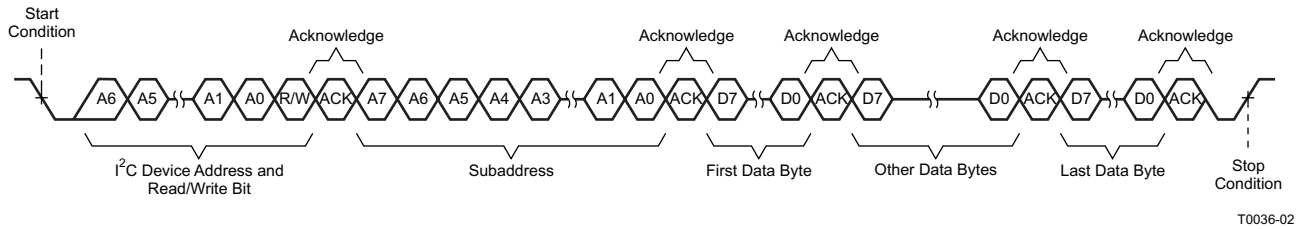


Figure 18. Sequential Write Transfer

Random Read

As shown in Figure 19, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the TAS5414A or TAS5424A responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5414A or TAS5424A address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5414A or TAS5424A again responds with an acknowledge bit. Next, the TAS5414A or TAS5424A transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

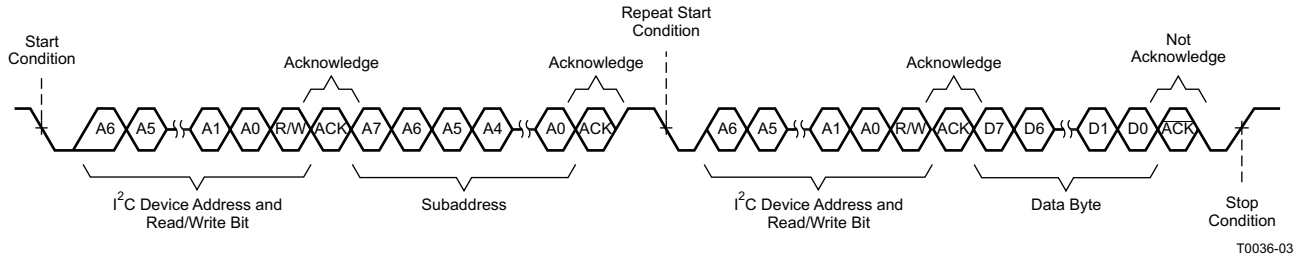


Figure 19. Random Read Transfer

Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS5414A or TAS5424A to the master device as shown in Figure 20. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I^2C subaddress by one. **Note:** The fault registers do not have sequential read capabilities.

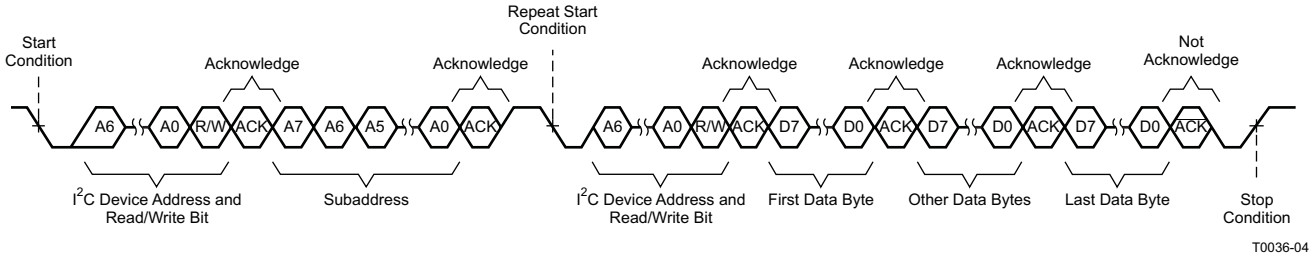


Figure 20. Sequential Read Transfer

Table 3. TAS5414A/5424 I²C Addresses

DESCRIPTION		FIXED ADDRESS					SELECTABLE WITH ADDRESS PIN		READ/WRITE BIT	I²C ADDRESS
		MSB	6	5	4	3	2	1	LSB	
TAS5414A/5424 0 (OSC MASTER)	I²C WRITE	1	1	0	1	1	0	0	0	0xD8
	I²C READ	1	1	0	1	1	0	0	1	0xD9
TAS5414A/5424 1 (OSC SLAVE1)	I²C WRITE	1	1	0	1	1	0	1	0	0xDA
	I²C READ	1	1	0	1	1	0	1	1	0xDB
TAS5414A/5424 2 (OSC SLAVE2)	I²C WRITE	1	1	0	1	1	1	0	0	0xDC
	I²C READ	1	1	0	1	1	1	0	1	0xDD
TAS5414A/5424 3 (OSC SLAVE3)	I²C WRITE	1	1	0	1	1	1	1	0	0xDE
	I²C READ	1	1	0	1	1	1	1	1	0xDF

Table 4. I²C Address Register Definitions

ADDRESS	R/W	REGISTER DESCRIPTION
0x00	R	Latched fault register 1, global and channel fault
0x01	R	Latched fault register 2, dc offset and overcurrent detect
0x02	R	Latched diagnostic register 1, load diagnostics
0x03	R	Latched diagnostic register 2, load diagnostics
0x04	R	External status register 1, temperature and voltage detect
0x05	R	External status register 2, Hi-Z and low-low state
0x06	R	External status register 3, mute and play modes
0x07	R	External status register 4, load diagnostics
0x08	R/W	External control register 1, channel gain select
0x09	R/W	External control register 2, dc offset reduction and current-limit select
0x0A	R/W	External control register 3, switching frequency and clip pin select
0x0B	R/W	External control register 4, load diagnostic, master mode select
0x0C	R/W	External control register 5, output state control
0x0D	R/W	External control register 6, output state control
0x0E	R/W	External control register 7, dc detect level select
0x0F	R/W	External control register 8, dc detect level select

Table 5. Fault Register 1 (0x00) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Overtemperature warning has occurred
–	–	–	–	–	–	1	–	DC offset has occurred in any channel
–	–	–	–	–	1	–	–	Overcurrent shutdown has occurred in any channel
–	–	–	–	1	–	–	–	Overtemperature shutdown has occurred
–	–	–	1	–	–	–	–	Charge pump undervoltage has occurred
–	–	1	–	–	–	–	–	AVDD, analog voltage, undervoltage has occurred
–	1	–	–	–	–	–	–	PVDD undervoltage has occurred
1	–	–	–	–	–	–	–	PVDD overvoltage has occurred

Table 6. Fault Register 2 (0x01) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Ovecurrent shutdown channel 1 has occurred
–	–	–	–	–	–	1	–	Overcurrent shutdown channel 2 has occurred

Table 6. Fault Register 2 (0x01) Protection (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	1	–	–	Overcurrent shutdown channel 3 has occurred
–	–	–	–	1	–	–	–	Overcurrent shutdown channel 4 has occurred
–	–	–	1	–	–	–	–	DC offset channel 1 has occurred
–	–	1	–	–	–	–	–	DC offset channel 2 has occurred
–	1	–	–	–	–	–	–	DC offset channel 3 has occurred
1	–	–	–	–	–	–	–	DC offset channel 4 has occurred

Table 7. Diagnostic Register 1 (0x02) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to ground channel 1 has occurred
–	–	–	–	–	–	1	–	Output short to PVDD channel 1 has occurred
–	–	–	–	–	1	–	–	Shorted load channel 1 has occurred
–	–	–	–	1	–	–	–	Open load channel 1 has occurred
–	–	–	1	–	–	–	–	Output short to ground channel 2 has occurred
–	–	1	–	–	–	–	–	Output short to PVDD channel 2 has occurred
–	1	–	–	–	–	–	–	Shorted load channel 2 has occurred
1	–	–	–	–	–	–	–	Open load channel 2 has occurred

Table 8. Diagnostic Register 2 (0x03) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to ground channel 3 has occurred
–	–	–	–	–	–	1	–	Output short to PVDD channel 3 has occurred
–	–	–	–	–	1	–	–	Shorted load channel 3 has occurred
–	–	–	–	1	–	–	–	Open load channel 3 has occurred
–	–	–	1	–	–	–	–	Output short to ground channel 4 has occurred
–	–	1	–	–	–	–	–	Output short to PVDD channel 4 has occurred
–	1	–	–	–	–	–	–	Shorted load channel 4 has occurred
1	–	–	–	–	–	–	–	Open load channel 4 has occurred

Table 9. External Status Register 1 (0x04) Fault Detection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults are present, default value
–	–	–	–	–	–	–	1	PVDD overvoltage fault is present
–	–	–	–	–	–	1	–	PVDD undervoltage fault is present
–	–	–	–	–	1	–	–	AVDD, analog voltage fault is present
–	–	–	–	1	–	–	–	Charge-pump voltage fault is present
–	–	–	1	–	–	–	–	Overtemperature shutdown is present
–	–	1	–	–	–	–	–	Overtemperature warning
–	1	1	–	–	–	–	–	Overtemperature warning level 1
1	0	1	–	–	–	–	–	Overtemperature warning level 2
1	1	1	–	–	–	–	–	Overtemperature warning level 3

Table 10. External Status Register 2 (0x05) Output State of Individual Channels

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	1	1	1	1	Output is in Hi-Z mode, not in low-low mode(1), default value
–	–	–	–	–	–	–	0	Channel 1 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	–	–	0	–	Channel 2 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	–	0	–	–	Channel 3 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	0	–	–	–	Channel 4 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	1	–	–	–	–	Channel 1 low-low mode (0 = not low-low, 1 = low-low)(1)
–	–	1	–	–	–	–	–	Channel 2 low-low mode (0 = not low-low, 1 = low-low)(1)
–	1	–	–	–	–	–	–	Channel 3 low-low mode (0 = not low-low, 1 = low-low)(1)
1	–	–	–	–	–	–	–	Channel 4 low-low mode (0 = not low-low, 1 = low-low)(1)

(1) *Low-low* is defined as both outputs actively pulled to ground.

Table 11. External Status Register 3 (0x06) Play and Mute Modes

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Mute mode is disabled, play mode disabled, default value, (Hi-Z mode)
–	–	–	–	–	–	–	1	Channel 1 play mode is enabled
–	–	–	–	–	–	1	–	Channel 2 play mode is enabled
–	–	–	–	–	1	–	–	Channel 3 play mode is enabled
–	–	–	–	1	–	–	–	Channel 4 play mode is enabled
–	–	–	1	–	–	–	–	Channel 1 mute mode is enabled
–	–	1	–	–	–	–	–	Channel 2 mute mode is enabled
–	1	–	–	–	–	–	–	Channel 3 mute mode is enabled
1	–	–	–	–	–	–	–	Channel 4 mute mode is enabled

Table 12. External Status Register 4 (0x07) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No channels are set in load diagnostics mode, default value
–	–	–	–	–	–	–	1	Channel 1 is in load diagnostics mode
–	–	–	–	–	–	1	–	Channel 2 is in load diagnostics mode
–	–	–	–	–	1	–	–	Channel 3 is in load diagnostics mode
–	–	–	–	1	–	–	–	Channel 4 is in load diagnostics mode
X	X	X	X	–	–	–	–	Reserved

Table 13. External Control Register 1 (0x08) Gain Select

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	0	1	0	1	0	1	0	Set gain for all channels to 26 dB, default value
–	–	–	–	–	–	0	0	Set channel 1 gain to 12 dB
–	–	–	–	–	–	0	1	Set channel 1 gain to 20 dB
–	–	–	–	–	–	1	1	Set channel 1 gain to 32 dB
–	–	–	–	0	0	–	–	Set channel 2 gain to 12 dB
–	–	–	–	0	1	–	–	Set channel 2 gain to 20 dB
–	–	–	–	1	1	–	–	Set channel 2 gain to 32 dB
–	–	0	0	–	–	–	–	Set channel 3 gain to 12 dB
–	–	0	1	–	–	–	–	Set channel 3 gain to 20 dB
–	–	1	1	–	–	–	–	Set channel 3 gain to 32 dB
0	0	–	–	–	–	–	–	Set channel 4 gain to 12 dB
0	1	–	–	–	–	–	–	Set channel 4 gain to 20 dB

Table 13. External Control Register 1 (0x08) Gain Select (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	1	–	–	–	–	–	–	Set channel 4 gain to 32 dB

Table 14. External Control Register 2 (0x09) DC Offset Reduction and Current Limit

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Enable dc offset reduction, set current limit to level 1
–	–	–	–	–	–	–	1	Disable channel 1 dc offset reduction
–	–	–	–	–	–	1	–	Disable channel 2 dc offset reduction
–	–	–	–	–	1	–	–	Disable channel 3 dc offset reduction
–	–	–	–	1	–	–	–	Disable channel 4 dc offset reduction
–	–	–	1	–	–	–	–	Set channel 1 current limit (0 = level 1, 1 = level 2)
–	–	1	–	–	–	–	–	Set channel 2 current limit (0 = level 1, 1 = level 2)
–	1	–	–	–	–	–	–	Set channel 3 current limit (0 = level 1, 1 = level 2)
1	–	–	–	–	–	–	–	Set channel 4 current limit (0 = level 1, 1 = level 2)

Table 15. External Control Register 3 (0x0A) Switching Frequency Select and Clip_OTW Configuration

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	1	1	0	1	Set f_S = 417 kHz, configure clip and OTW, 45° phase, disable hard stop
–	–	–	–	–	–	0	0	Set f_S = 500 kHz
–	–	–	–	–	–	1	0	Set f_S = 357 kHz
–	–	–	–	–	–	1	1	Invalid frequency selection (do not set)
–	–	–	–	0	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin for tweeter detect only
–	–	–	–	0	1	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin for clip detect only
–	–	–	–	1	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin for overtemperature warning only
–	–	–	1	–	–	–	–	Enable hard-stop mode
–	–	1	–	–	–	–	–	Set f_S to a 180° phase difference between adjacent channels
X	X	–	–	–	–	–	–	Reserved

Table 16. External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	1	0	0	0	0	0	0	Disable load diagnostics and dc detect SD, master mode
–	–	–	–	–	–	–	1	Enable channel 1, load diagnostics
–	–	–	–	–	–	1	–	Enable channel 2, load diagnostics
–	–	–	–	–	1	–	–	Enable channel 3, load diagnostics
–	–	–	–	1	–	–	–	Enable channel 4, load diagnostics
–	–	–	1	–	–	–	–	Enable dc detect shutdown on all channels
–	–	1	–	–	–	–	–	Enable tweeter-detect mode
–	0	–	–	–	–	–	–	Enable slave mode (external oscillator must be provided)
X	–	–	–	–	–	–	–	Reserved

Table 17. External Control Register 5 (0x0C) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	1	1	1	1	1	All channels, Hi-Z, mute, reset disabled
–	–	–	–	–	–	–	0	Set channel 1 to mute mode, non-Hi-Z
–	–	–	–	–	–	0	–	Set channel 2 to mute mode, non-Hi-Z
–	–	–	–	–	0	–	–	Set channel 3 to mute mode, non-Hi-Z
–	–	–	–	0	–	–	–	Set channel 4 to mute mode, non-Hi-Z

Table 17. External Control Register 5 (0x0C) Output Control (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	0	–	–	–	–	Set non-Hi-Z channels to play mode, (unmute)
–	1	1	–	–	–	–	–	Reserved
1	–	–	–	–	–	–	–	Reset device (I^2C does not respond with an ACK)

Table 18. External Control Register 6 (0x0D) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Low-low state disabled all channels
–	–	–	–	–	–	–	1	Set channel 1 to low-low state
–	–	–	–	–	–	1	–	Set channel 2 to low-low state
–	–	–	–	–	1	–	–	Set channel 3 to low-low state
–	–	–	–	1	–	–	–	Set channel 4 to low-low state
X	X	X	X	–	–	–	–	Reserved

Table 19. External Control Register 7 (0x0E) Positive DC Detect Threshold Selection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	0	0	0	1	1	1	0	Default positive dc detect value
0	1	1	0	0	1	0	1	Minimum positive dc detect value
X	X	X	X	X	X	X	X	See Figure 11 to set positive dc detect value
1	1	0	0	1	0	1	1	Maximum positive dc detect value

Table 20. External Control Register 8 (0x0F) Negative DC Detect Threshold Selection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	1	1	1	1	0	1	Default negative dc detect value
0	1	1	0	0	1	0	1	Minimum negative dc detect value
X	X	X	X	X	X	X	X	See Figure 12 to set negative dc detect value
0	0	0	0	0	0	0	0	Maximum negative dc detect value

Hardware Control Pins

The TAS5414A and TAS5424A incorporate four discrete hardware pins for real-time control and indication of device status.

$\overline{\text{FAULT}}$ pin: This active-low, open-drain output pin indicates the presence of a fault condition that requires the TAS5414A and TAS5424A to go automatically into the Hi-Z mode or standby mode. When this pin is asserted high, the device has acted to protect itself and the system from potential damage. The exact nature of the fault can be read via I^2C with the exception of faults that are the result of PVDD voltage excursions above 25 Vdc or below 5.5 Vdc. In these instances, the device goes into standby mode and the I^2C bus is no longer operational. However, the fault is still indicated due to the fact that the $\overline{\text{FAULT}}$ pin is open-drain and active-high.

$\overline{\text{CLIP\_OTW}}$ pin: The function of this active-high pin is configured by the user to indicate one of the following conditions: overtemperature warning, the detection of clipping, or the logical OR of both of these conditions. The configuration is selected via I^2C. During tweeter detect diagnostics, this pin also is asserted when a tweeter is present.

$\overline{\text{MUTE}}$ pin: This active-low pin is used for hardware control of the mute/unmute function for all four channels. Capacitor C_{MUTE} is used to control the time constant for the gain ramp needed to produce a pop- and click-free mute function. For pop- and click-free operation, the mute function should be implemented through I^2C commands. The use of a hard mute with an external transistor does not ensure pop- and click-free operation, and is not recommended unless an *emergency hard mute* function is required in case of a loss of I^2C control. The value of C_{MUTE} must be 330 nF for proper pop- and click-free operation.

$\overline{\text{STANDBY}}$ pin: When this active-low pin is asserted, the device goes into a complete shutdown, and current draw is limited to 2 μA, typical. This is pin typically asserted when the car ignition is in the off position. It can also be used to shut down the device rapidly when certain operating conditions are violated. All I^2C register content is lost when this pin is asserted. The I^2C bus goes into the high-impedance state when the $\overline{\text{STANDBY}}$ pin is asserted.

EMI Considerations

Automotive level EMI performance depends on both careful integrated circuit design and good system level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the TAS5414A and TAS5424A design.

The TAS5414A and TAS5424A have minimal parasitic inductances due to the short leads on the PSOP3 package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel of the TAS5414A and TAS5424A also operates at a different phase. The phase between channels is I^2C selectable to either 45° or 180°, to reduce EMI caused by high-current switching. The TAS5414A and TAS5424A incorporate patent-pending circuitry that optimizes output transitions that cause EMI.

AM Radio EMI Reduction

To reduce interference in the AM radio band, the TAS5414A and TAS5424A have the ability to change the switching frequency via I^2C commands. The recommended frequencies are listed in Table 21. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio. To function properly, AM avoidance requires the use of a 20-kΩ, 1% tolerance Rext resistor.

Table 21. Recommended Switching Frequencies for AM Mode Operation

US		EUROPEAN	
AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)
		522-540	417
540–917	500	540–914	500
917–1125	417	914–1122	417
1125–1375	500	1122–1373	500
1375–1547	417	1373–1548	417
1547–1700	357	1548–1701	357

Operating States

The operating regions, or states, of the TAS5414A and TAS5424A are depicted in the following tables.

Table 22. Operating States and Supplies

STATE NAME	OUTPUT FETS	CHARGE PUMP	OSCILLATOR	I^2C	AVDD and DVDD
STANDBY	Hi-Z, floating	Stopped	Stopped	Stopped	OFF
Hi-Z	Hi-Z, weak pulldown	Active	Active	Active	ON
Mute	Switching at 50%	Active	Active	Active	ON
Normal operation	Switching with audio	Active	Active	Active	ON

Table 23. Global Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED/ SELF-CLEARING
POR	Voltage fault	All	$\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Self-clearing
UV		Hi-Z, mute, normal	I^2C + $\overline{\text{FAULT}}$ pin		Hi-Z	
CP UV					Hi-Z	
OV					Hi-Z	
Load dump		All	$\overline{\text{FAULT}}$ pin		Standby	
OTW	Thermal warning	Hi-Z, mute, normal	I^2C + $\overline{\text{CLIP\_OTW}}$ pin	None	None	Self-clearing
OT	Thermal fault	Hi-Z, mute, normal	I^2C + $\overline{\text{FAULT}}$ pin	Hard mute	Standby	Self-clearing

Table 24. Channel Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED/ SELF-CLEARING
Open/short diagnostic	Diagnostic	Hi-Z (I^2C activated)	I^2C	None	None	Latched
Clipping online	Warning	Normal	$\overline{\text{CLIP\_OTW}}$ pin	None	None	Self-clearing
CBC load current limit	Online protection	Mute, normal	$\overline{\text{CLIP\_OTW}}$ pin	Current limit	Start OC timer	Self-clearing
OC fault	Output channel fault	Mute, normal	I^2C + $\overline{\text{FAULT}}$ pin	Hard mute	Hi-Z	Latched
DC detect		Normal	I^2C + $\overline{\text{FAULT}}$ pin	Hard mute	Hi-Z	Latched

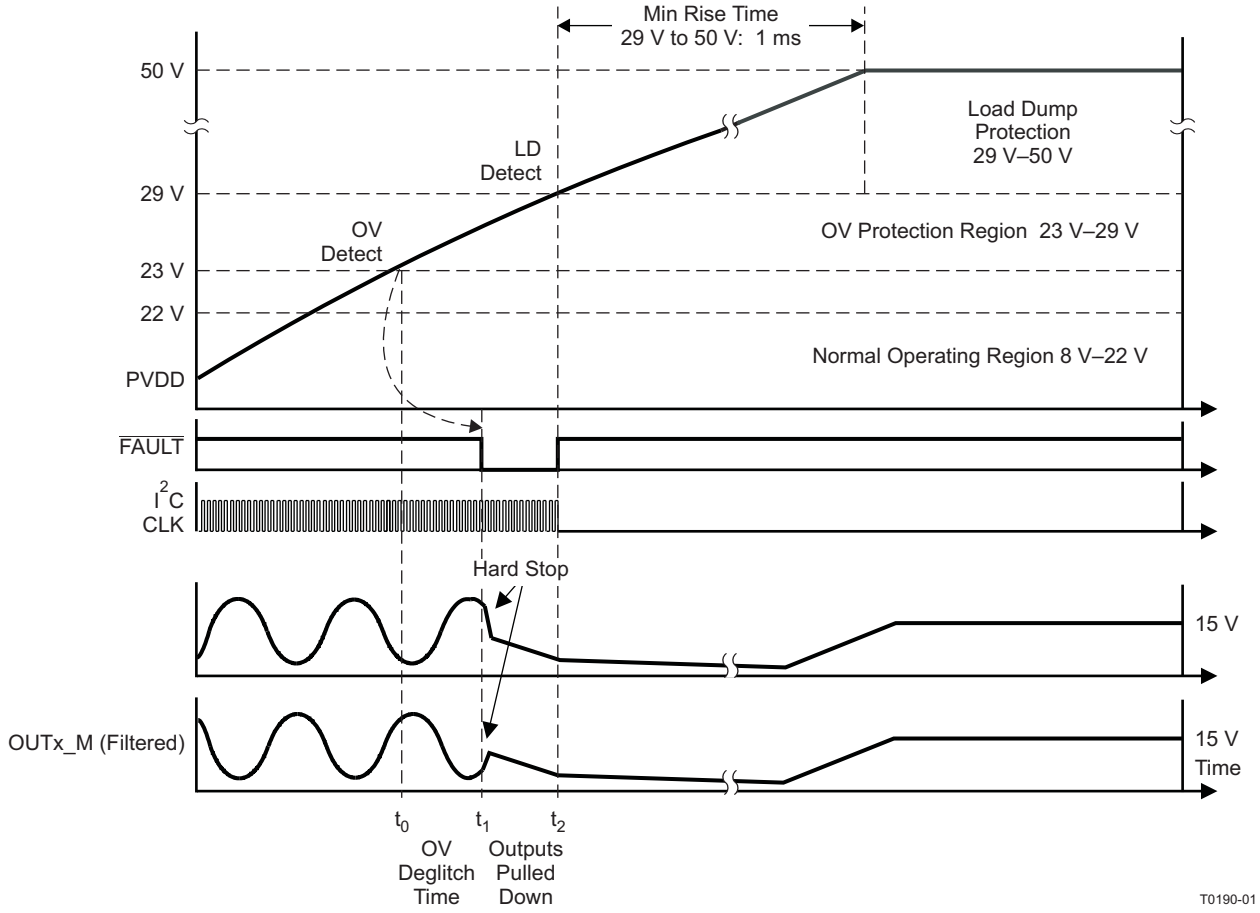


Figure 21. Sequence of Events for Supply Transition Out of Normal Operating Region

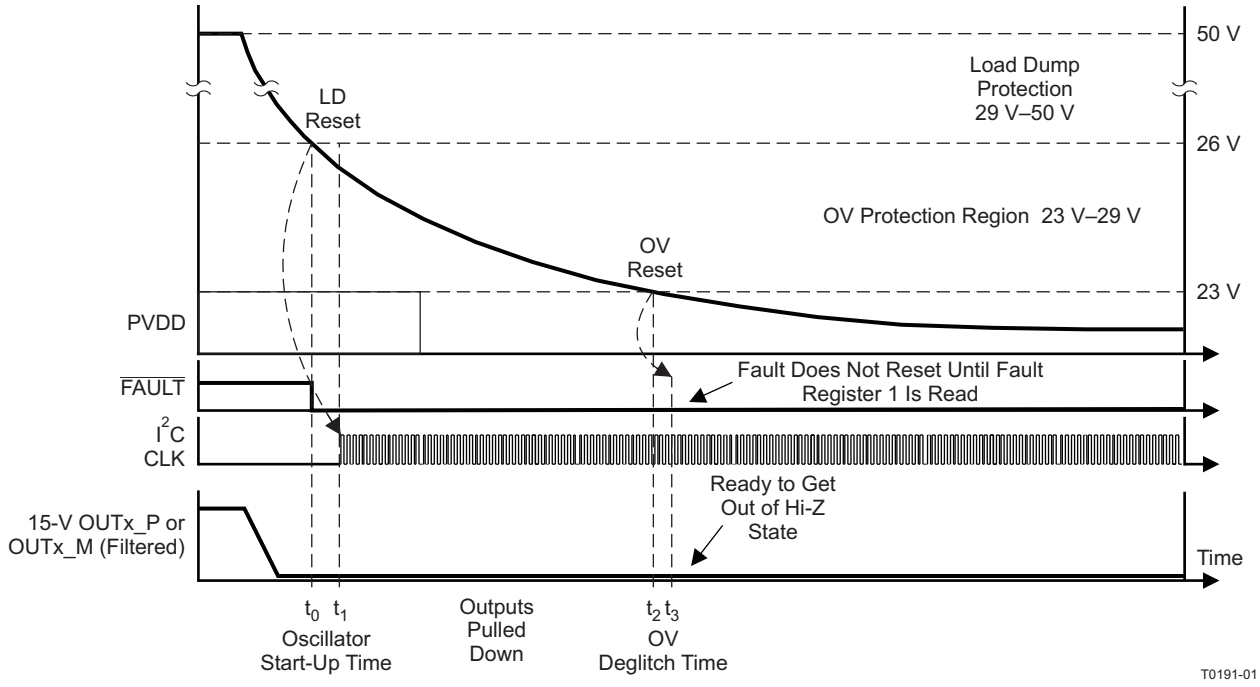


Figure 22. Sequence of Events for Supply Transition Back Into Normal Operating Region

Power Shutdown and Restart Sequence Control

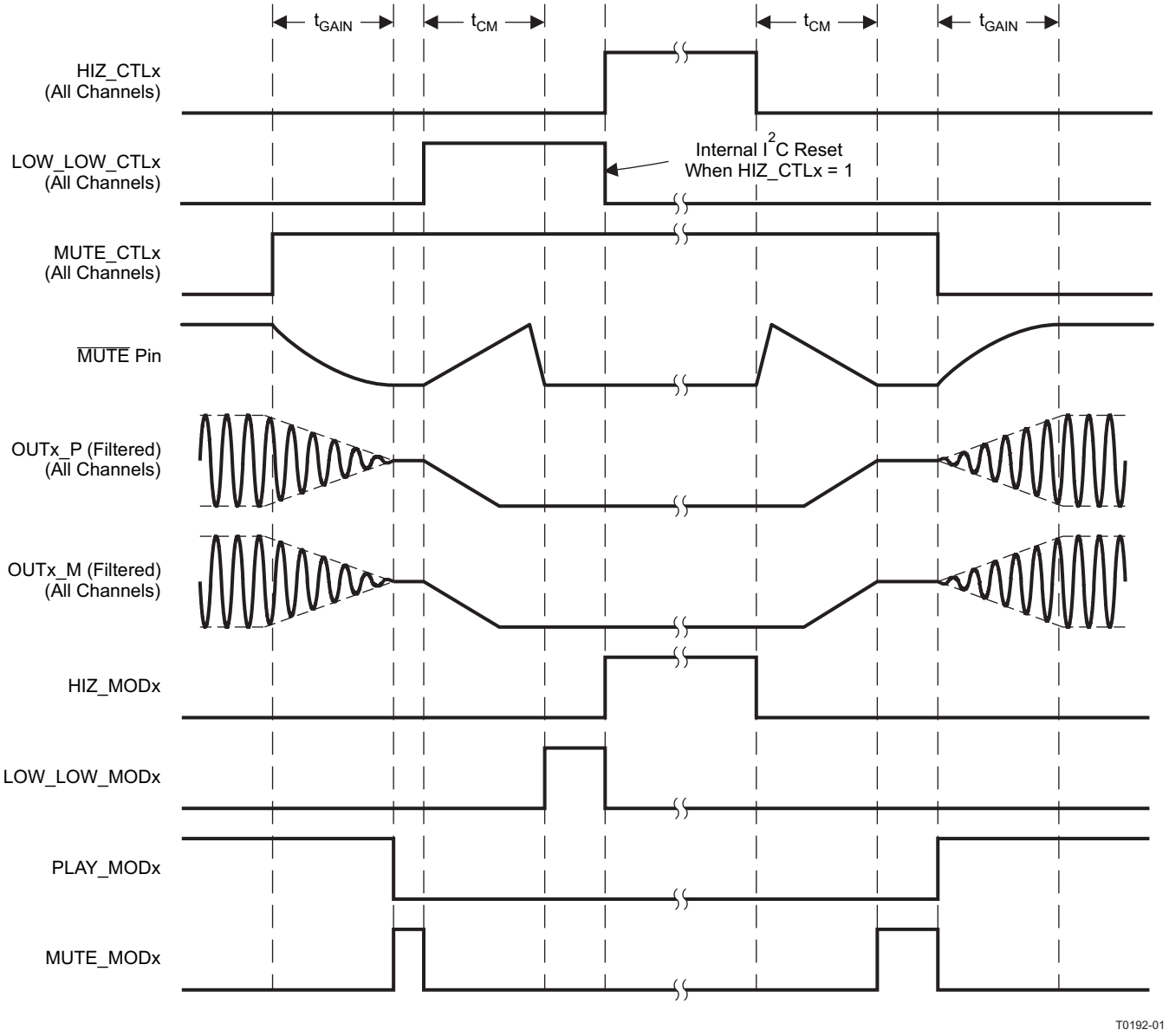


Figure 23. Click- and Pop-Free Shutdown and Restart Sequence Timing Diagram With Four Channels Sharing the Mute Pin

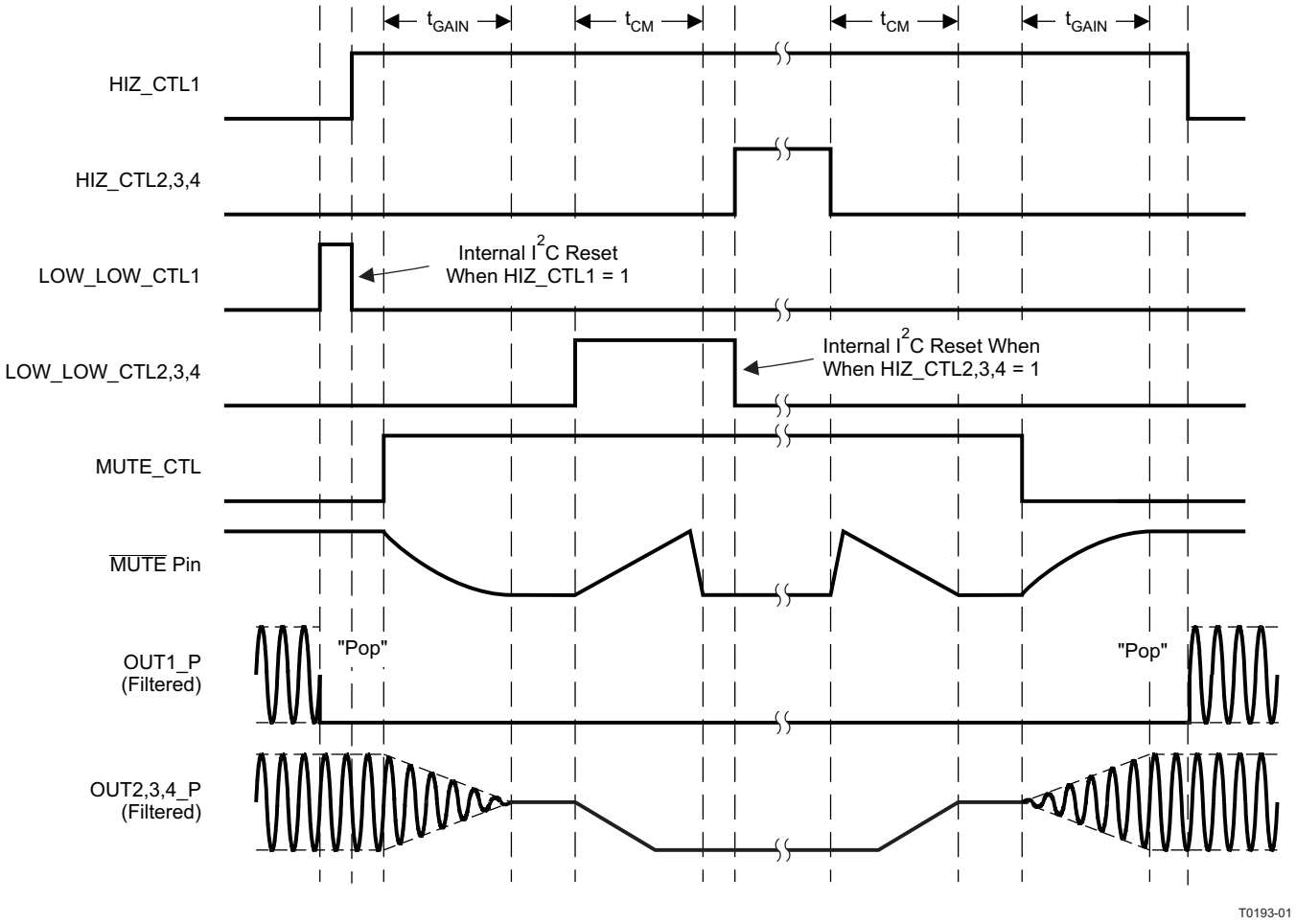


Figure 24. Individual Channel Shutdown and Restart Sequence Timing Diagram

Latched Fault Shutdown and Restart Sequence Control

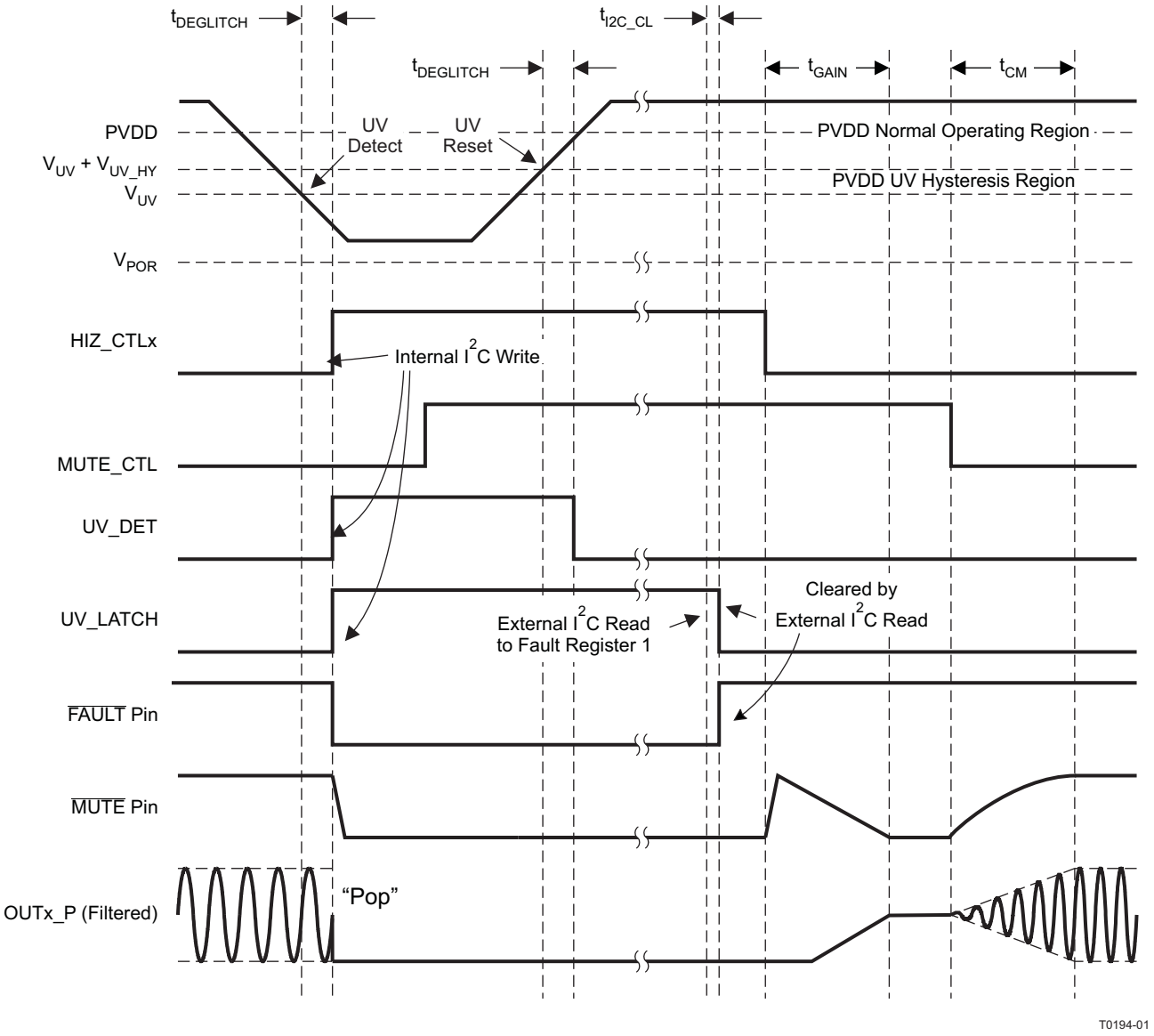


Figure 25. Latched Global Fault Shutdown and Restart Timing Diagram (UV Shutdown and Recovery)

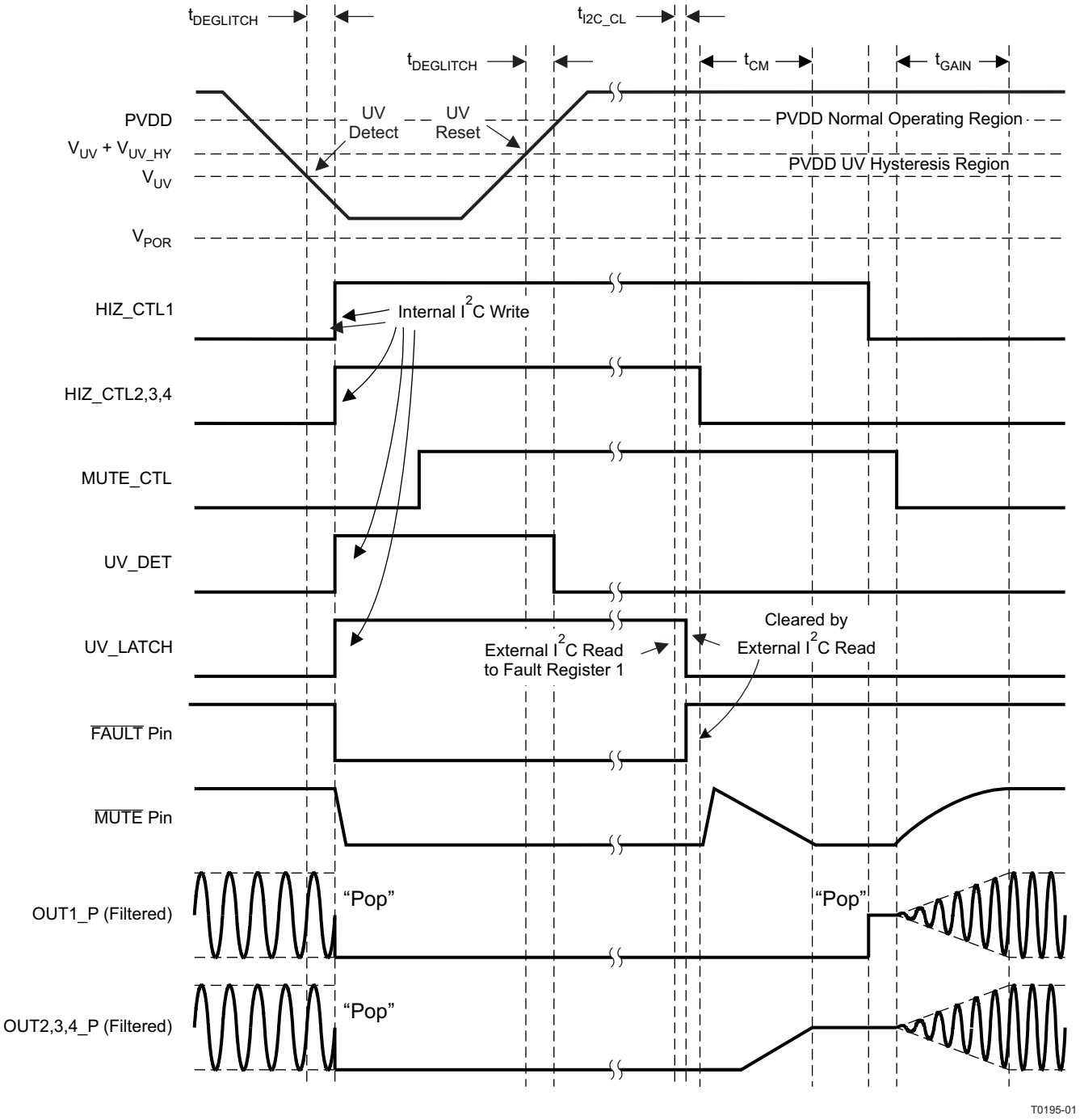


Figure 26. Latched Global Fault Shutdown and Individual Channel Restart Timing Diagram (UV Shutdown and Recovery)

APPLICATION INFORMATION

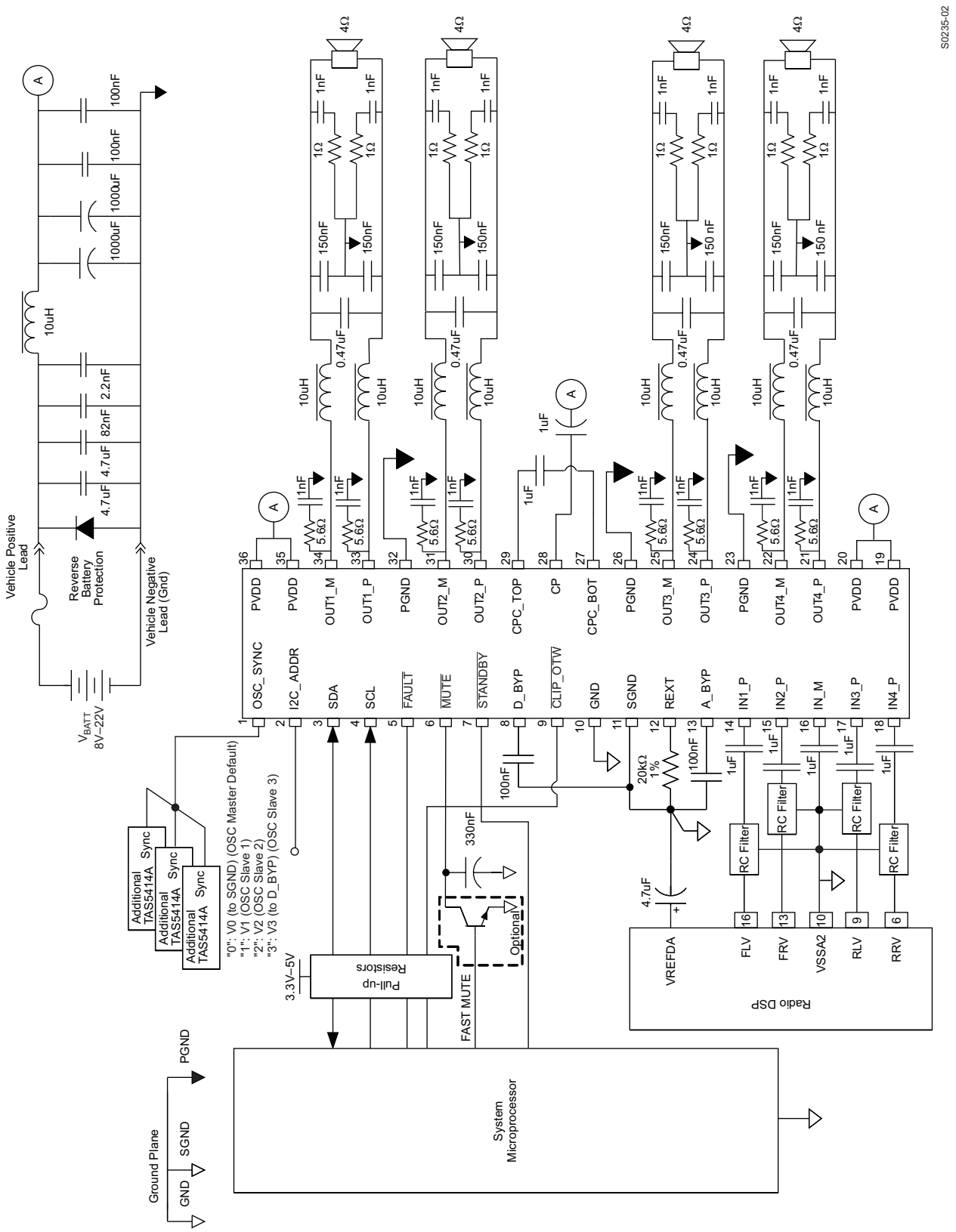


Figure 27. TAS5414A Application Schematic

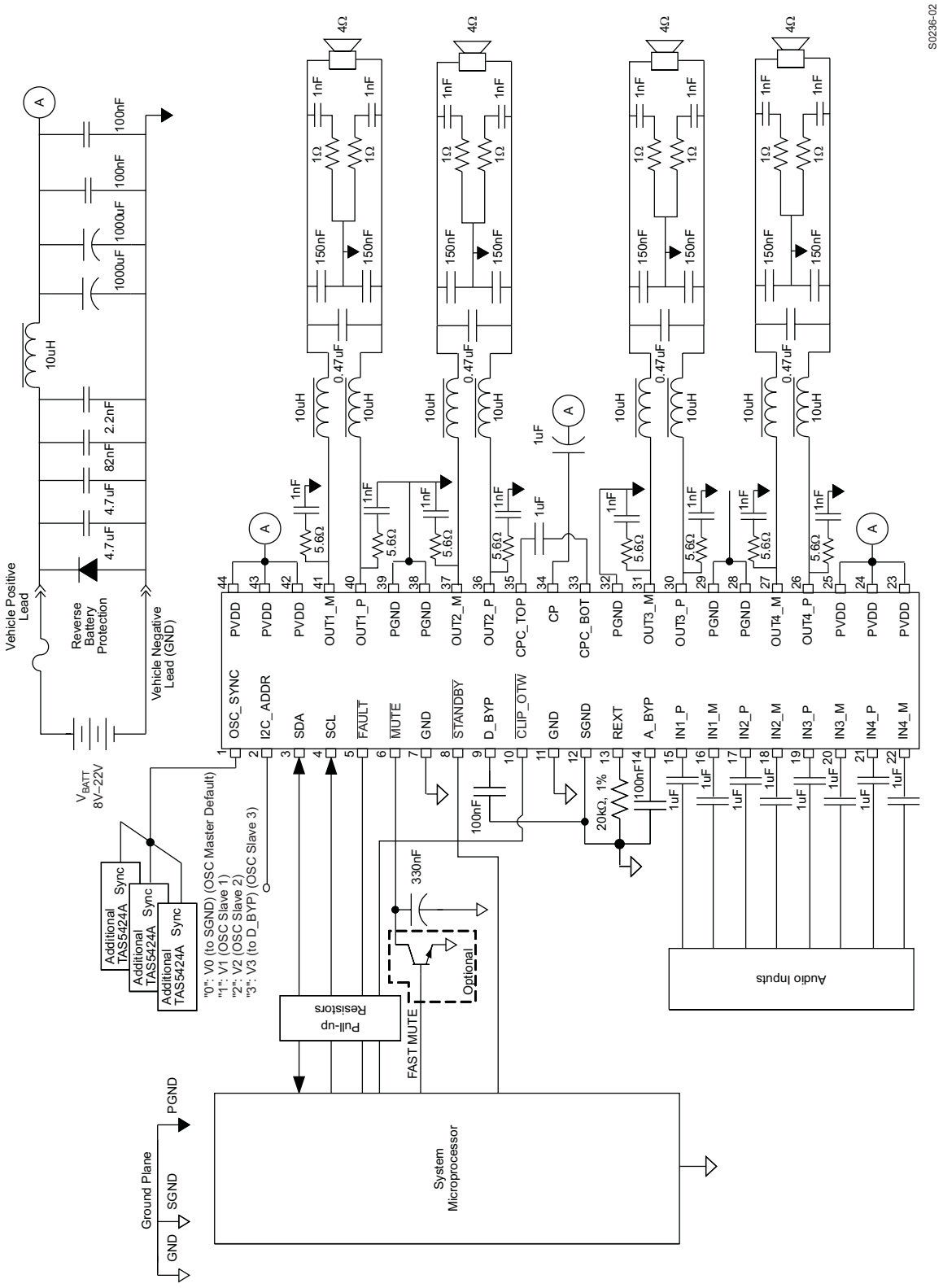


Figure 28. TAS5424A Typical Application Schematic

Parallel Operation (PBTL)

TAS5414A and TAS5424A can be used to drive four 4Ω loads, two 2Ω loads, or even one 1Ω load by paralleling BTL channels on the load side of the LC output filter. For parallel operation, identical I^2C settings are required for any two paralleled channels (especially gain and current-limit settings) in order to have reliable system performance and evenly dissipated power on multiple channels. Having identical gain and current-limit settings can also prevent energy feeding back from one channel to the other. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, etc.) should be sent to the paralleled channels at the same time. Load diagnostic is also supported for parallel connection. Paralleling on the TAS5414A and TAS5424A side of the LC output filter is not supported, and can result in device failure.

DEMODULATION FILTER DESIGN

The TAS5414A and TAS5424A amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal. The main purpose of the demodulation filter is to attenuate the high-frequency components of the output signals that are out of the audio band. Design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the device THD+N specification, the selection of the inductors used in the output filter should be carefully considered. The rule is that the inductance should remain stable within the range of peak current seen at maximum output power and deliver approximately 5 μH of inductance at 16 A. If this rule is observed, the TAS5414A and TAS5424A should not have distortion issues due to the output inductors. Another parameter to be considered is the idle-current loss in the inductor. This can be measured or specified as inductor dissipation (D). The target specification for dissipation is less than 0.05. If the dissipation factor is above this value, idle current increases. In general, 10-μH inductors suffice for most applications. The frequency response of the amplifier is slightly altered by the change in output load resistance; however, unless tight control of frequency response is necessary (better than 0.5 dB), it is not necessary to deviate from 10 μH.

THERMAL INFORMATION

The thermally augmented package provided with the TAS5414A and TAS5424A is designed to interface directly to heat sinks using a thermal interface compound (for example, Artic Silver, Ceramique thermal compound.) The heat sink then absorbs heat from the ICs and couples it to the local air. If louvers or fans are supplied, this process can reach equilibrium and heat can be continually removed from the ICs. Because of the efficiency of the TAS5414A and TAS5424A, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W or °C-mm^2/W). The area thermal resistance of the example thermal grease with a 0.001-inch (0.0254-mm) thick layer is about 0.007°C-in^2/W (4.52°C-mm^2/W). The approximate exposed heat slug size is as follows:

TAS5424A, 44-pin PSOP3	0.124 in^2 (80 mm^2)
TAS5414A, 36-pin PSOP3	0.124 in^2 (80 mm^2)
TAS5414A, TAS5424A, 64-pin QFP.....	0.099 in^2 (64 mm^2)

Dividing the example thermal grease area resistance by the area of the heat slug gives the actual resistance through the thermal grease for both parts:

TAS5424A, 44-pin PSOP3	0.06°C/W
TAS5414A, 36-pin PSOP3	0.06°C/W
TAS5414A, TAS5424A, 64-pin QFP.....	0.07°C/W

The thermal resistance of thermal pads is generally considerably higher than a thin thermal grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance generally is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus, for a single monaural channel in the IC, the system $R_{\theta JA} = R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

The following table indicates modeled parameters for one TAS5414A or TAS5424A IC on a heat sink. The junction temperature is set at 115°C in both cases while delivering 20 Wrms per channel into 4-Ω loads with no clipping. It is assumed that the thermal grease is about 0.001 inches (0.0254 mm) thick.

Device	TAS5414A, 36-Pin PSOP3
Ambient temperature	25°C
Power to load	20 W × 4
Power dissipation	1.90 W × 4
ΔT inside package	7.6°C
ΔT through thermal grease	0.46°C
Required heatsink thermal resistance	10.78°C/W
Junction temperature	115°C
System $R_{\theta JA}$	11.85°C/W
$R_{\theta JA}$ × power dissipation	90°C

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TAS5414ATDKDMQ1	ACTIVE	SSOP	DKD	36	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATDKDMQ1G4	ACTIVE	SSOP	DKD	36	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATDKDQ1	ACTIVE	SSOP	DKD	36	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATDKDQ1G4	ACTIVE	SSOP	DKD	36	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATDKDRMQ1	ACTIVE	SSOP	DKD	36	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATDKDRMQ1G4	ACTIVE	SSOP	DKD	36	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATDKDRQ1	ACTIVE	SSOP	DKD	36	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATDKDRQ1G4	ACTIVE	SSOP	DKD	36	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5414ATPHDMQ1	ACTIVE	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5414ATPHDMQ1G4	ACTIVE	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5414ATPHDQ1	ACTIVE	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5414ATPHDQ1G4	ACTIVE	HTQFP	PHD	64	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5414ATPHDRMQ1	ACTIVE	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5414ATPHDRMQ1G4	ACTIVE	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5414ATPHDRQ1	ACTIVE	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5414ATPHDRQ1G4	ACTIVE	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS5424ATDKDMQ1	ACTIVE	SSOP	DKD	44	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATDKDMQ1G4	ACTIVE	SSOP	DKD	44	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATDKDQ1	ACTIVE	SSOP	DKD	44	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATDKDQ1G4	ACTIVE	SSOP	DKD	44	29	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATDKDRMQ1	ACTIVE	SSOP	DKD	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATDKDRMQ1G4	ACTIVE	SSOP	DKD	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATDKDRQ1	ACTIVE	SSOP	DKD	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATDKDRQ1G4	ACTIVE	SSOP	DKD	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR
TAS5424ATPHDMQ1	PREVIEW	HTQFP	PHD	64	90	TBD	Call TI	Call TI

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TAS5424ATPHDQ1	PREVIEW	HTQFP	PHD	64	90	TBD	Call TI	Call TI
TAS5424ATPHDRMQ1	PREVIEW	HTQFP	PHD	64	1000	TBD	Call TI	Call TI
TAS5424ATPHDRQ1	PREVIEW	HTQFP	PHD	64	1000	TBD	Call TI	Call TI

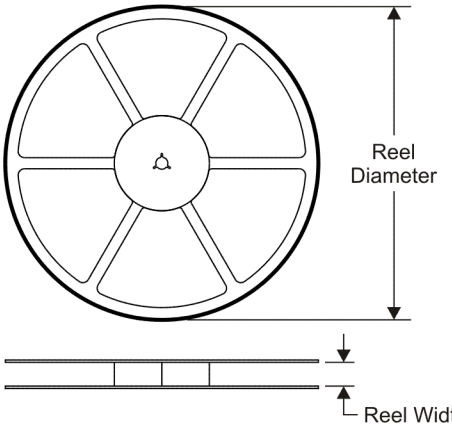
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

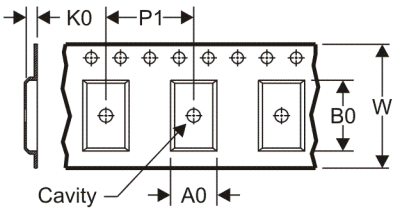
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

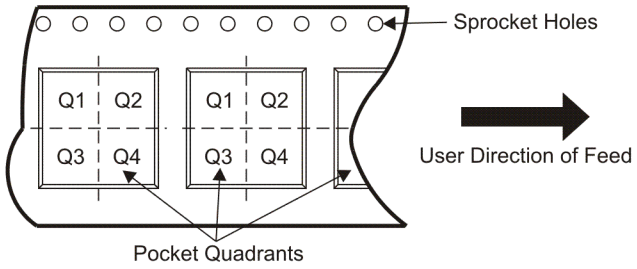


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

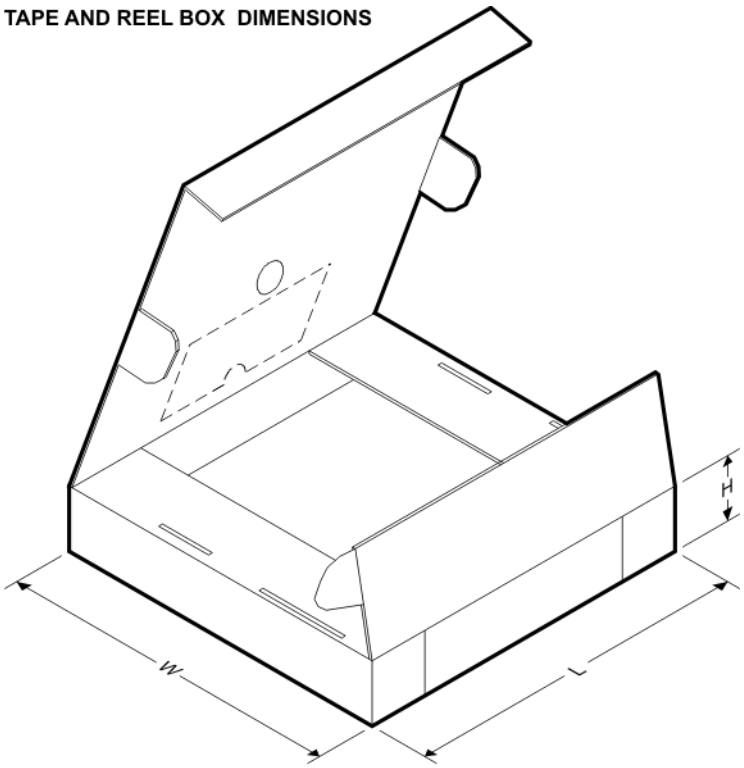
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5414ATDKDRMQ1	SSOP	DKD	36	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1
TAS5424ATDKDRMQ1	SSOP	DKD	44	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1
TAS5424ATDKDRQ1	SSOP	DKD	44	500	330.0	24.4	14.7	16.4	4.0	20.0	24.0	Q1

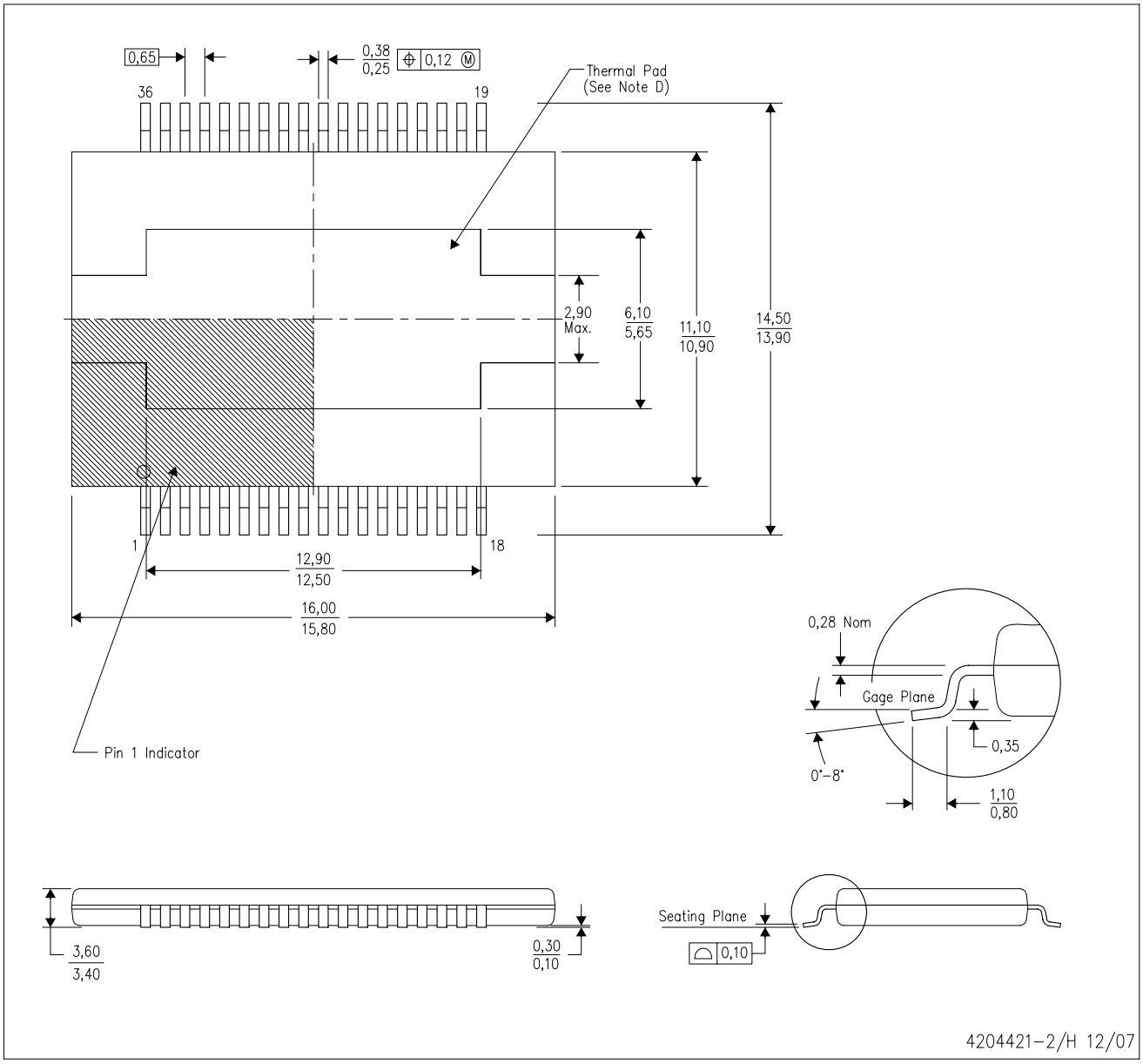
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

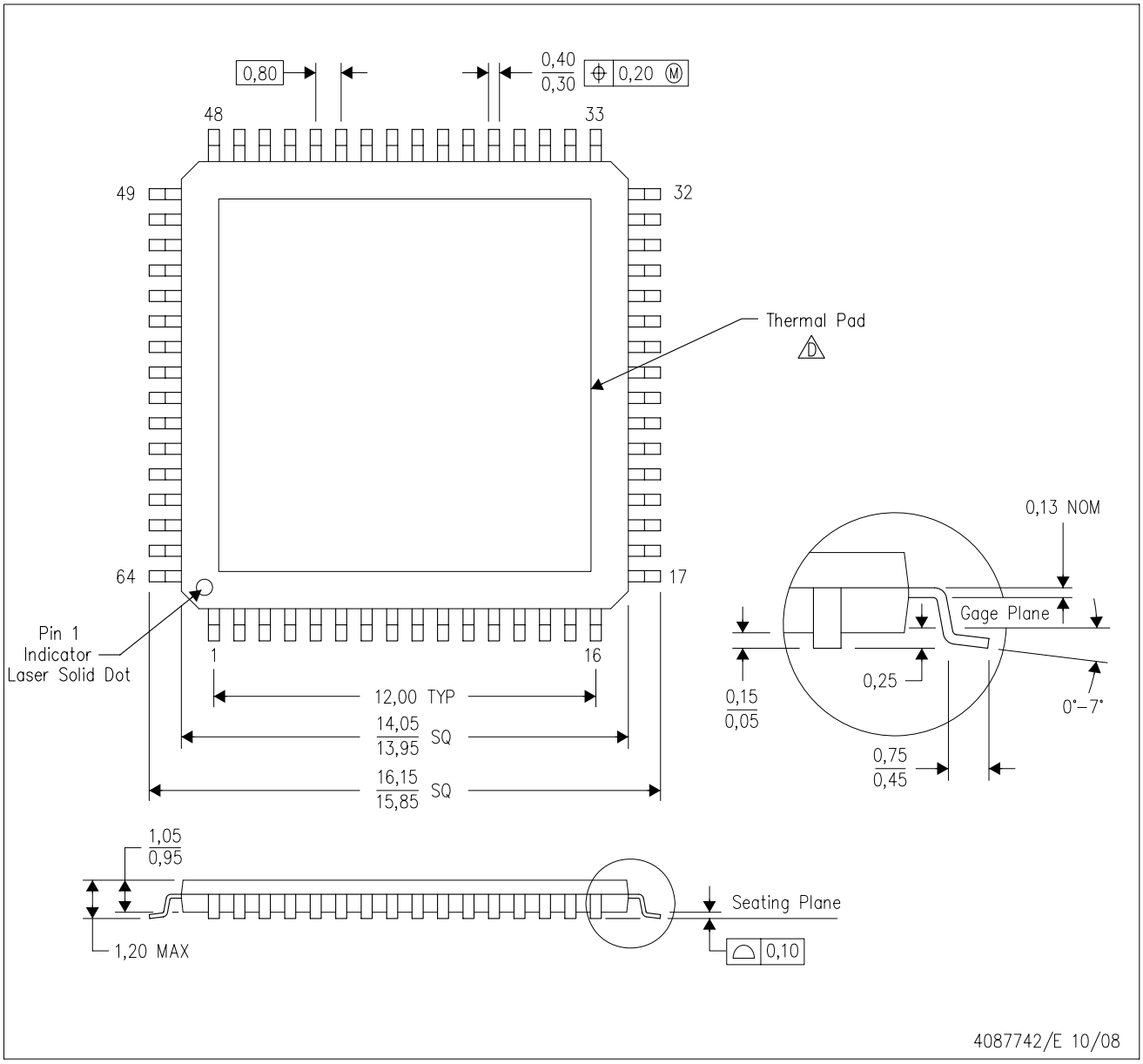
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5414ATDKDRMQ1	SSOP	DKD	36	500	346.0	346.0	41.0
TAS5424ATDKDRMQ1	SSOP	DKD	44	500	346.0	346.0	41.0
TAS5424ATDKDRQ1	SSOP	DKD	44	500	346.0	346.0	41.0

DKD (R–PDSO–G36) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15mm.
D. The package thermal performance is optimized for conductive cooling with attachment to an external heat sink. See the product data sheet for details regarding the exposed thermal pad dimensions.

PHD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

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RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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